Low-Noise DC Amplifier Board for Power Detector Signal Conditioning

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1.0	07.05.2010	J.A. Lopez-Perez	First version

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1 Introduction

This report shows the construction and characterization of a low-noise DC amplifier for the conditioning of low voltage signals provided by power detectors.

Power detectors are used in radioastronomy receivers to measure the total power of the signal collected by the radiotelescope within receiver's band. These are called **continuum measurements**. In addition, they are used to monitor the signal level in the receiver's band, which is usefull for receiver monitor and control.

The output voltage of a power detector, which is proportional to the power of its input signal (quadratic law), is very weak. This kind of signals need to be amplified to a voltage range that fits with the input of digital acquisition systems. Table 1 shows typical parameters of commercial power detectors.

For instance, a signal of -30 dBm at the input of the Herotek DT2018 will provide an output of 0.7 mV only, which is too low to be sampled by an analogue-to-digital converter (ADC).

In this text, the circuit schematic will be shown first, together with the part list. Then, the printed circuit board (PCB) layers will be presented and some pictures of two of these units will be shown, too. Finally, voltage gain and noise measurements on these units will be given.

Table 1: Parameters of some commercial power detectors.

Model Part Nr.	**Frequency Range**	**Sensitivity**	**Tangencial Sensitivity**[1]	**Output Polarity**
Herotek DT2018	2.0 - 18.0 GHz	700 mV/mW	-50 dBm	Negative
Agilent 8472B-002-003	0.01 - 18.0 GHz	500 mV/mW	-45 dBm	Positive
Agilent 8471D-102-103	100 KHz - 2 GHz	500 mV/mW	-35 dBm	Positive

2 Circuit Schematic

Figure 1 shows a plot of the schematic circuit. The circuit is based on a design from Y. Bortolotti for IRAM Plateau de Bure millimeter wave receivers, with some modifications to allow the input of either positive or negative signals.

[1] TSS based on 2 MHz video bandwidth and 2 dB amplifier NF (Herotek) and 3dB amplifier (Agilent).

The first part is an instrumentation low noise amplifier, with a voltage gain of 500. After this, the circuit has a low-pass filter (R7-C1), with a cut-off around 200Hz, and a second low noise amplifier with a voltage gain equal to 2. Thus, the overall voltage gain is 1000.

Resistors R3 and R4 can be changed to modify the value of the gain. High accuracy resistor can be used to set a particular gain value. By its side, potentiometer ADJ1 is needed to cancel out any ouput offset voltage.

Positive and negative voltage regulators are also provided for the power supply of the amplifiers.

Figures 2 and 3 show the top and bottom copper layer of the printed circuit board, respectively. By its side, figure 4 shows the top silk layer for component identification.

The look of the board, without components, can be seen in figure 5, while figure 6 shows the final board after component integration. Two boards have been integrated, one for negative input signals (sn01) and the other for positive input signals (sn02).

3 Measurements

The following parameters have been measured for each board:

- DC voltage gain
- AC voltage gain versus input frequency
- Output noise with short-circuit input
- Output noise with open-circuit input

3.1 DC Voltage gain

The DC voltage gain was measured with the help of a variable DC power supply at the input and two multimeters, one at the input and one at the output. The output offset voltage was cancelled previously. This was done by shorting the input and turning the potentiometer ADJ1 until zero is read in the output multimeter display.

The input and output values of these measurements can be seen in table 2 for each board. These values are represented grafically in figures 7 and 8. The measurements have been fitted with straigth lines in the linear region to compute the DC voltage gain, which results in a value of -978.17 for sn01 and 977.32 for sn02. It has to be noted that the slope for sn01 is negative because it is prepared to accept negative input signals.

Table 2: DC voltage gain measurements.

Vin$_{sn01}$ (mV)	**Vout$_{sn01}$ (V)**	**Vin$_{sn02}$ (mV)**	**Vout$_{sn02}$ (V)**
-1.24	1.215	1.45	1.441
-2.32	2.283	2.52	2.491
-3.39	3.33	3.59	3.527
-4.46	4.37	4.67	4.590
-5.27	5.17	5.49	5.385
-6.35	6.22	6.54	6.422
-7.42	7.27	7.63	7.49
-8.51	8.33	8.70	8.53
-9.30	9.11	9.51	9.31
-10.37	10.15	10.58	10.36
-11.44	11.18	11.66	11.26
-12.53	11.27	12.72	11.27
-13.33	11.27	13.53	11.27
-14.39	11.27	14.60	11.27
-15.47	11.27	15.68	11.27

3.2 AC Voltage gain

The AC voltage gain was measured with the help of the Agilent 35670A FFT dynamic analyzer in its transfer function measurement mode. In both cases, the source generator was set to 1 mVp-p. The results are given in figures 9 and 10, where amplitude and phase of the voltage gain are shown. The voltage gain is near to 60dB, which implies a value close to 1000, and the -3dB cut-off frequency is around 100Hz, imposed by the low-pass filter (R7-C1), and a 180^o shift can be seen among the phases of each board, due to the fact that one is ready for negative input voltages and the other for positive ones.

3.3 Output noise with short-circuit at the input

The output noise was measured with the help of the Agilent 35670A FFT dynamic analyzer in its spectrum analyzer mode. The power spectrum of the output signal, with no input signal (short circuit in this case) is computed and presented for each board. The analyzer makes normalization to give values in $\mu V_{rms}/\sqrt{Hz}$.

Figures 11 and 12 show the spectrum of the output noise with short circuit at the input of the boards. At 100 Hz, the noise is 2.7 $\mu V_{rms}/\sqrt{Hz}$ and 3.1 $\mu V_{rms}/\sqrt{Hz}$ for sn01 and sn02, respectively. To refer this value to the input noise, we must divide by the gain at 100 Hz, which will be approximated by 1000. Then, the input noise at 100Hz will be $2.7 nV_{rms}/\sqrt{Hz}$ and $3.1 nV_{rms}/\sqrt{Hz}$. These values are in agreement with the input voltage noise specification of the AD625 instrumentation amplifier, whose values is $4\ nV_{rms}/\sqrt{Hz}$.

3.4 Output noise with open-circuit at the input

This case was measured to have an indication of the noise when the input of the board is loaded with a high impedance.

Figures 13 and 14 show the spectrum of the output noise with an open circuit at the input of the boards. At 100Hz, the noise is 31.5 $\mu V_{rms}/\sqrt{Hz}$ and 17.7 $\mu V_{rms}/\sqrt{Hz}$ for sn01 and sn02, respectively. To refer this value to the input noise, we must divide by the gain at 100Hz, which will be approximated by 1000. Then, the input noise at 100 Hz will be 31.5 $nV_{rms}/\sqrt{Hz}$ and 17.7 $nV_{rms}/\sqrt{Hz}$.

4 Conclusions

A board has been successfully integraded and tested for the low noise amplification of the low-level signals from power detectors. The offset of the board can be compensated and the gain can be selected by appropiate selection of a couple of resistors. In addition, the board can be configured for either positive of negative input signals. Finally, the cut-off frequency can be modified by changing the values of the low-pass filter (R7-C1), too.

Acknowledgments

The author wishes to thank the help provided by C. Almendros and S. Henche for their work during the routing of the PCB board, the assembly and soldering and the measurements of DC gain.

The help provided by J.D. Gallego in the measurement of AC gain and noise is also appreciated.

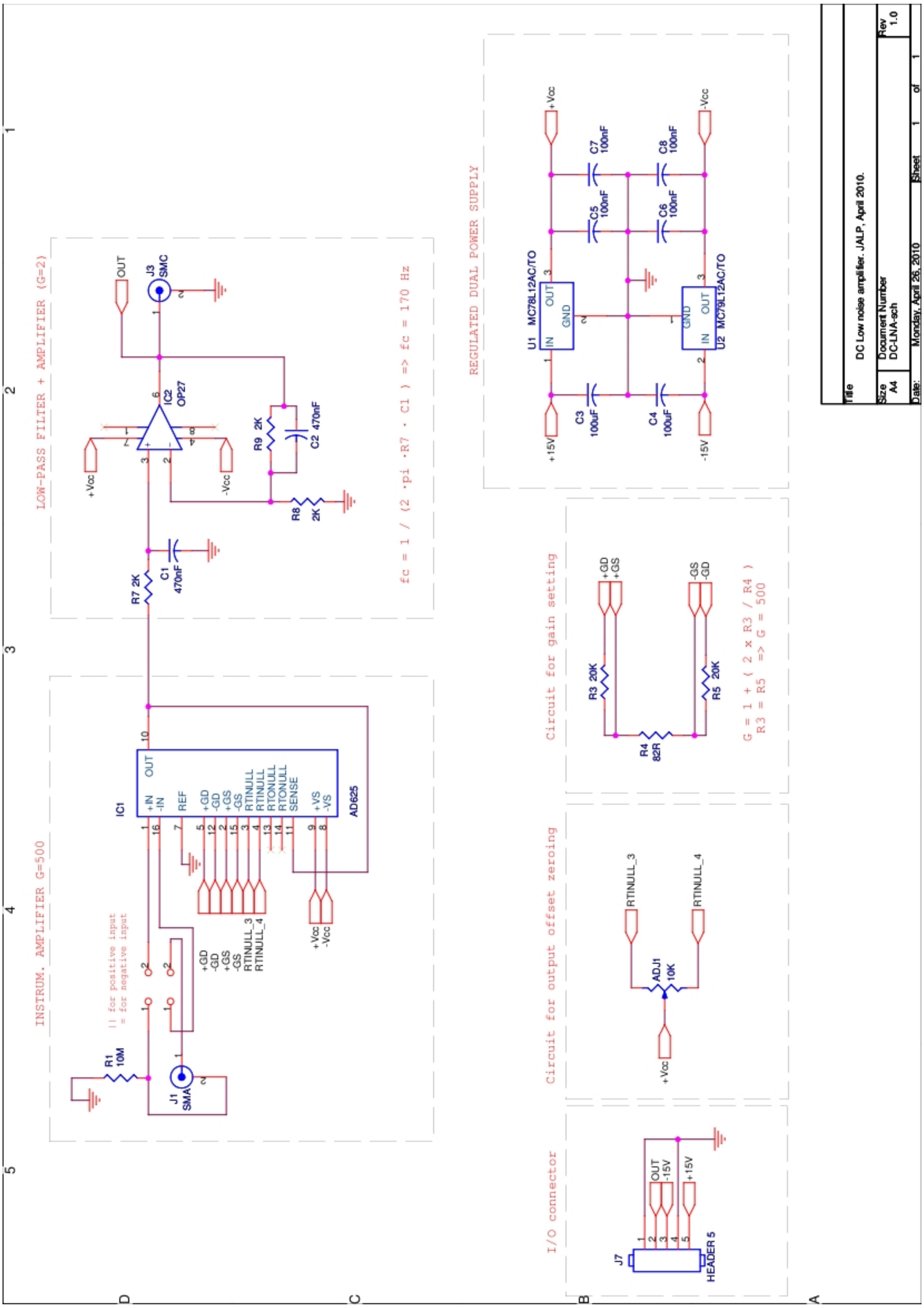

Figure 1: Low noise DC amplifier schematic circuit.

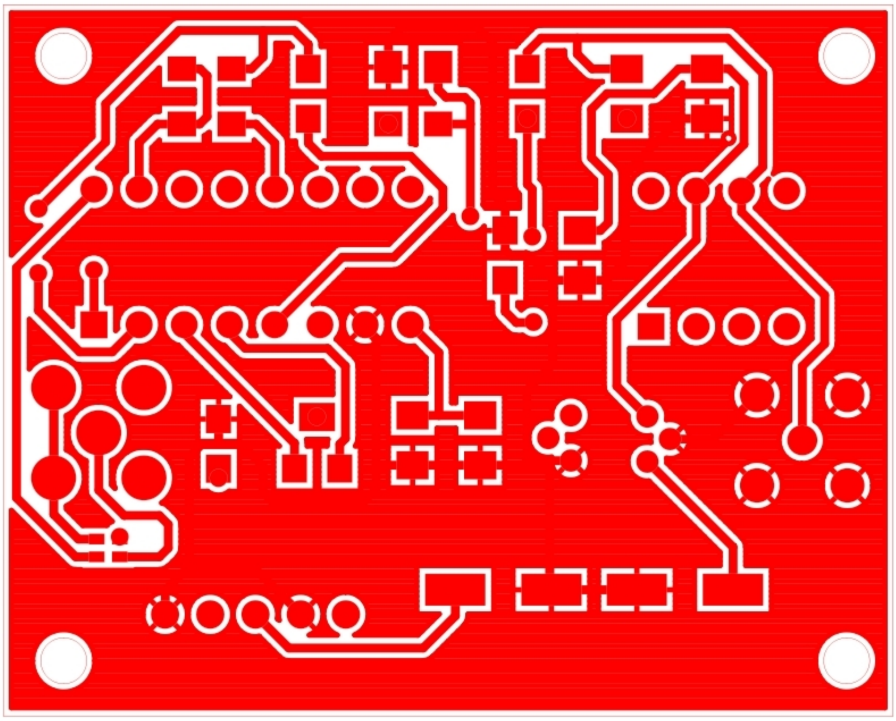

Figure 2: PCB top layer.

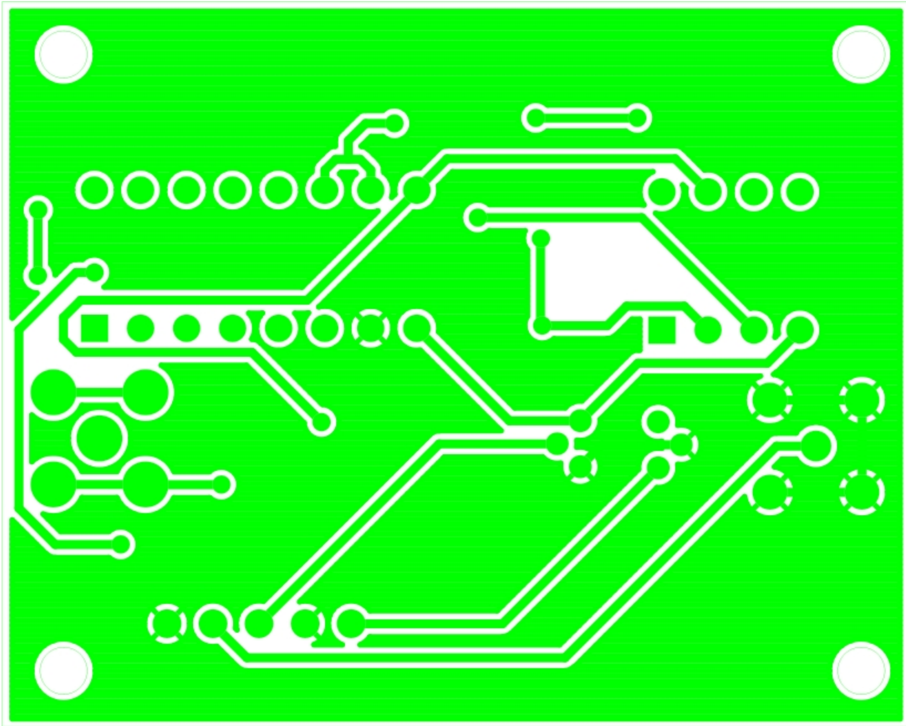

Figure 3: PCB bottom layer.

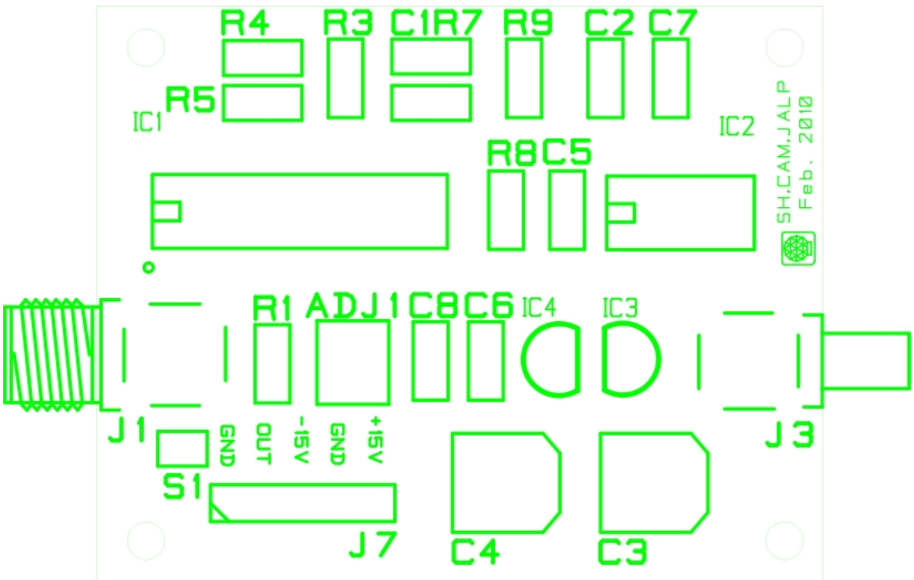

Figure 4: PCB top silk layer.

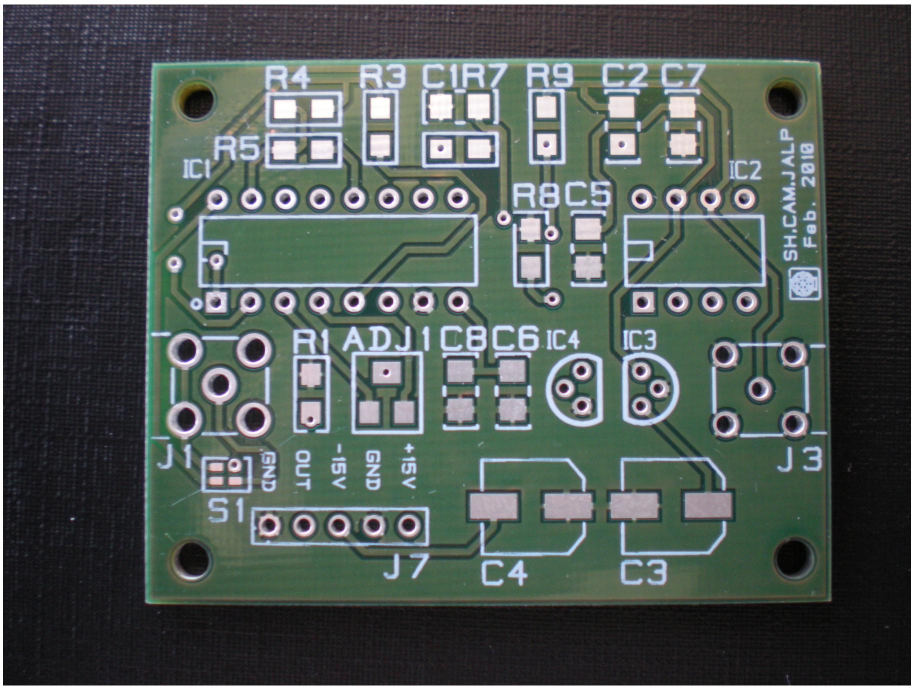

Figure 5: Empty low noise DC amplifier board.

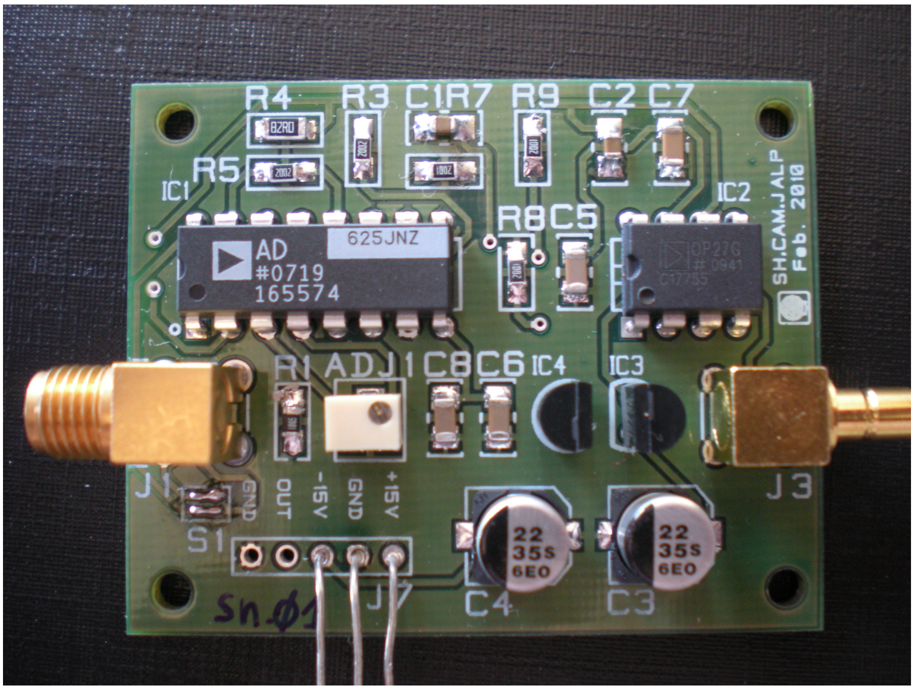

Figure 6: Integrated low noise DC amplifier board.

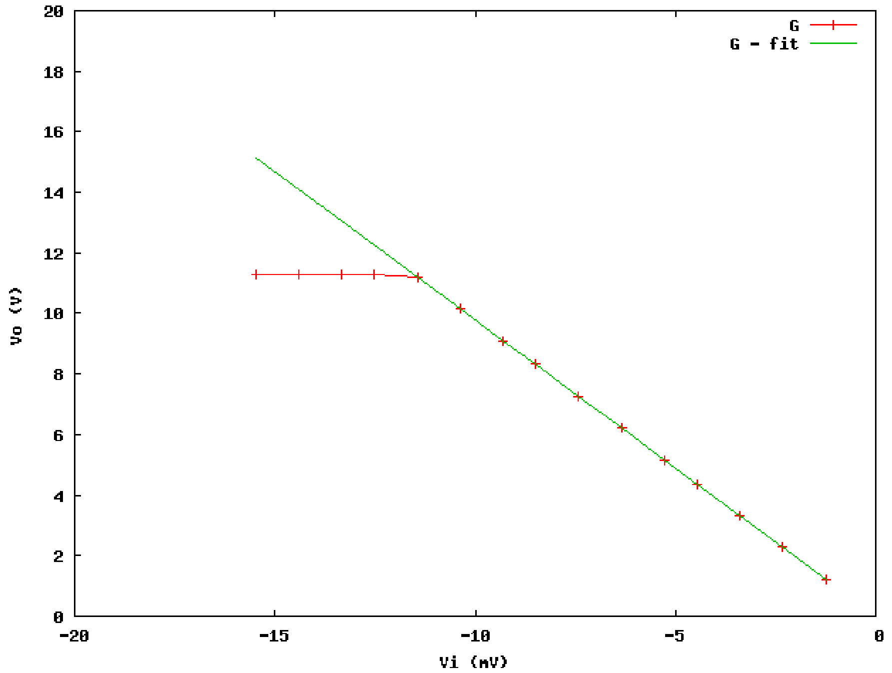

Figure 7: DC voltage gain of board sn01.

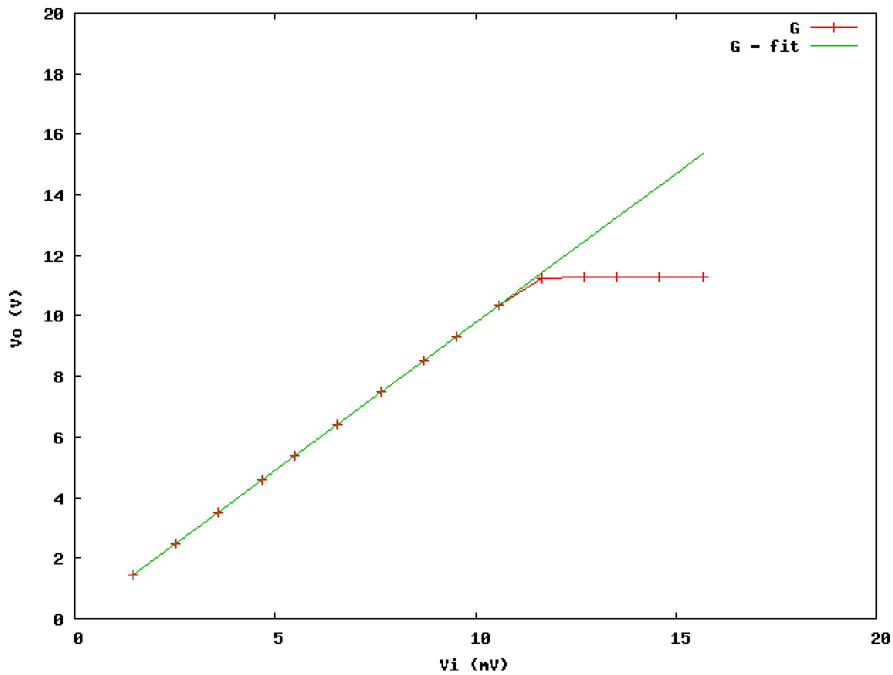

Figure 8: DC voltage gain of board sn02.

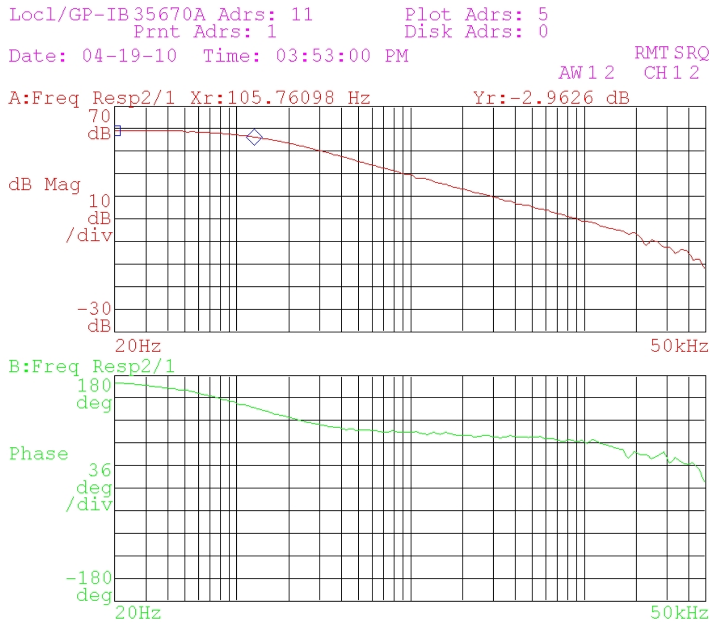

Figure 9: AC voltage gain of board sn01.

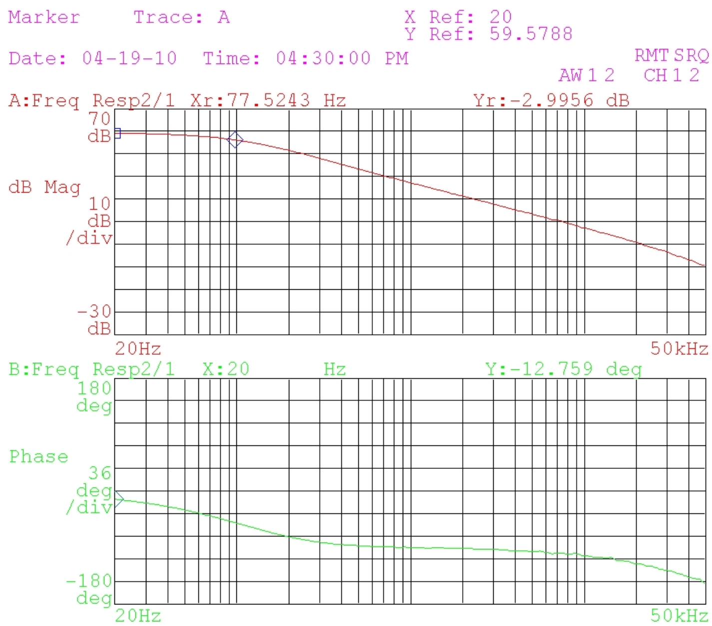

Figure 10: AC voltage gain of board sn02.

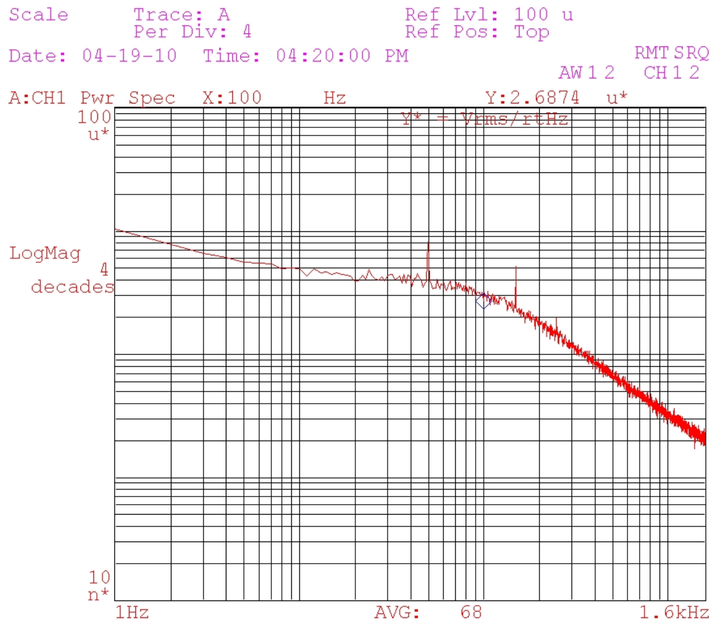

Figure 11: Ouput noise with short-circuit input of board sn01.

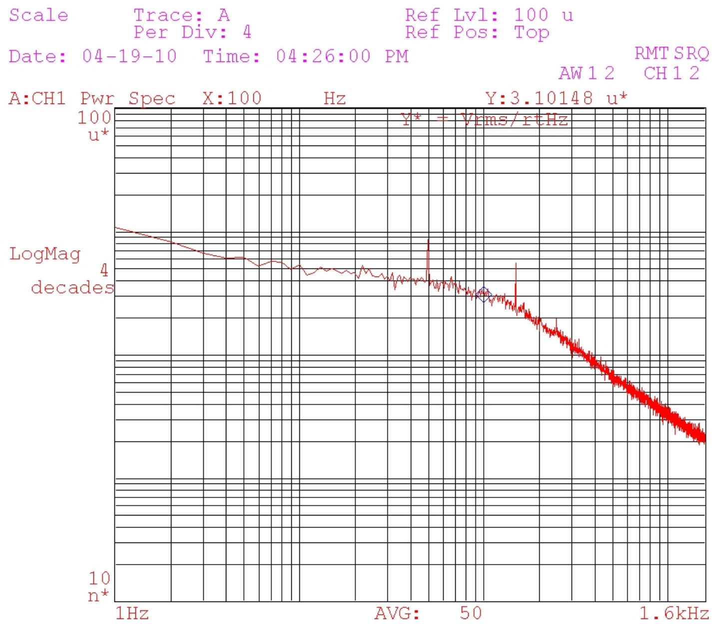

Figure 12: Ouput noise with short-circuit input of board sn02.

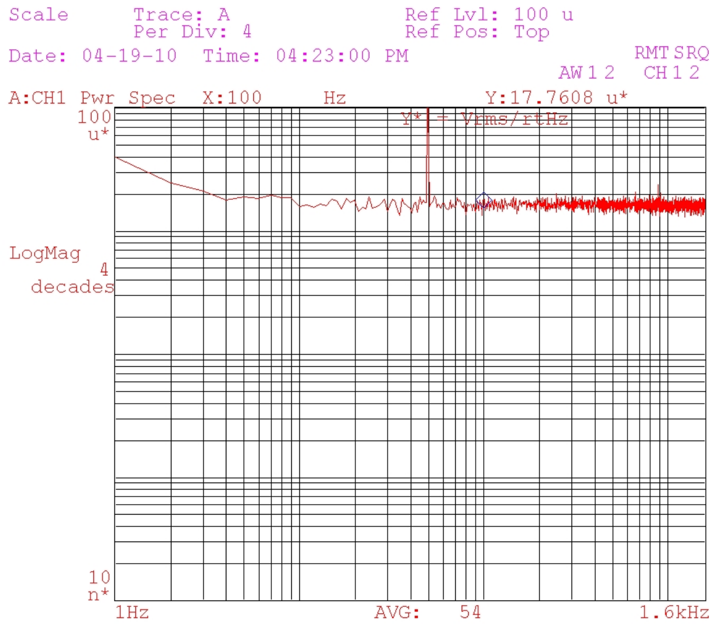

Figure 13: Ouput noise with open-circuit input of board sn01.

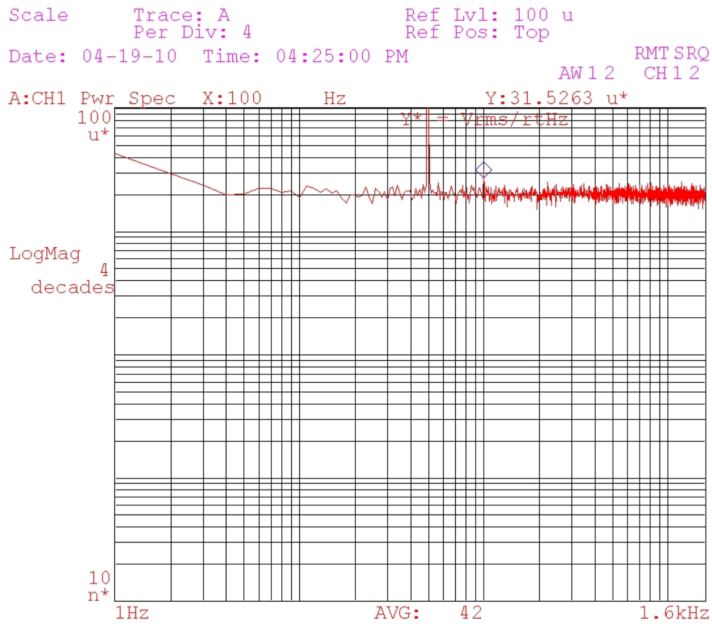

Figure 14: Ouput noise with open-circuit input of board sn02.