Circuito de control del atenuador programable

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Descripción de la funcionalidad del circuito de control del atenuador programable incluido en el submódulo de ruido. Construcción de la placa e integración en el submódulo, incluido en el receptor de 22 GHz de la antena de 40 m del CAY. Esquemas y layout. Pruebas realizadas. Hojas de características de los componentes.

1 Introducción

Esta placa forma parte del submódulo de ruido, integrado en el módulo de FI, del receptor de 22 GHz de la antena de 40 m. en el CAY.

Su propósito es controlar la programación del atenuador 84904K de Agilent, incluido en dicho submódulo y cuyo objetivo es permitir la selección de una potencia adecuada de ruido introducido en el sistema.

Existen 4 bits del bus de control del módulo destinados al control de la atenuación programada, y a partir de estos el circuito diseñado genera las señales de control adecuadas para el atenuador.

El diagrama de bloques del submódulo de ruido se encuentra en el Anexo A.- Esquema del submódulo de ruido.

El esquema eléctrico del circuito se ha realizado con OrCAD y se adjunta en el Anexo B.- Esquema eléctrico del circuito, mientras que el layout de la placa construida se ha realizado con CADStar y puede encontrarse en el Anexo C.- Layout de la placa.

2 Descripción del circuito

2.1 Señales de entrada

Las señales de entrada de la placa son:

- Señal de alimentación de 5 V (conector *J5V*); necesaria para alimentar el CI SN74LS04 (componente *U1*), y los drivers DS75452 (componentes *U2, U3, U4, U5*).
- Señal de alimentación de 15 V (conector *J15V*); necesaria para proporcionar las señales de control del atenuador programable y la señal de salida que servirá para la alimentación de éste.
- *IN1..4*: bits de control con niveles TTL (conectores *J1..4)*, a partir de los cuales se generan las señales con niveles de 0 y 15 V, que actúan sobre las celdas del atenuador programable. Estas señales proceden del módulo de control del receptor, y llegan a la placa a través del bus de control.

2.2 Señales de salida

Las señales de salida de la placa son:

- Señal de alimentación de 15 V (conector *J015V*) y masa; obtenida tras el paso de la señal de entrada de 15 V por un filtro EMI, para así eliminar posibles señales interferentes que puedan influir en el comportamiento del circuito. Se utilizará para la alimentación del atenuador programable.
- *THRU1..4* y *ATT1..4*: Señales generadas para el control de las celdas del atenuador programable (conectores *J11, J21, J31, J41*, y *J12, J22, J32, J42* respectivamente). Son señales con niveles de 0 y 15 V.

2.3 El Atenuador Programable 84904K de Agilent

El circuito diseñado genera señales de control para el atenuador programable 84904K Opt.015 Opt.004 de Agilent, que está integrado en el submódulo de ruido.

Se trata de un atenuador con 4 celdas de atenuación, de 1, 2, 4 y 4 dB respectivamente. De este modo pueden programarse atenuaciones de 0 a 11 dB, con pasos de 1 dB.

En la *Tabla 1* se especifican las celdas que deben ser activadas para obtener cada una de las atenuaciones que es posible programar:

	Atenuación											
Secciones	**0 dB**	**1 dB**	**2 dB**	**3 dB**	**4 dB**	**5 dB**	**6 dB**	**7 dB**	**8 dB**	**9 dB**	**10dB**	**11dB**
Sección 1 (1 dB)		X		X		X		X		X		X
Sección 2 (2 dB)			X	X			X	X			X	X
Sección 3 (4 dB)					X	X	X	X	X	X	X	X
Sección 4 (4 dB)									X	X	X	X

Tabla 1 – Relación entre celdas activadas y atenuación conseguida en el atenuador programable 84904K Opt015 Opt004 de Agilent

Cada una de las celdas está controlada por dos señales (*"Thru Line"* y *"Att Card"*), en las que deben establecerse niveles de 0 y 15V (al tratarse del modelo de atenuador Opt.015, la tensión de señal admitida como nivel alto comprende de 13 V a 22 V). Estas señales son excluyentes, esto es, el par de señales de control de una misma celda nunca deben encontrarse a un mismo nivel.

Las señales son activas a nivel bajo, de modo que si la señal *Thru* se encuentra a nivel bajo y la señal *Att* de la misma celda está a nivel alto, la celda en cuestión no actuará sobre la señal, que pasará sin ser atenuada; por otro lado, si se tiene un nivel alto en la señal *Thru* y un nivel bajo en la señal *Att*, la celda actuará sobre la señal, atenuándola como corresponde.

El atenuador es controlado a través de un bus terminado en un conector DIP de 10 pines. La correspondencia de estos pines con las señales de control y alimentación se presenta en la siguiente tabla:

Celda (atenuación)	**Señal**	**Pin del conector DIP**	**Color del cable del conector DIP**
Sección 1 (att = 1 dB)	Thru1	1	Marrón
	Att1	2	Rojo
Sección 2 (att = 2 dB)	Thru2	5	Verde
	Att2	8	Gris
Sección 3 (att = 4 dB)	Thru3	4	Amarillo
	Att3	9	Blanco
Sección 4 (att = 4 dB)	Thru4	6	Azul
	Att4	7	Violeta
	Alimentación 15 V	10	Negro
	GND	3	Naranja

Tabla 2 – Correspondencia entre las señales de salida de la placa y los pines del conector DIP de 10 pines para el control del atenuador programable 84904K Opt015 Opt004 de Agilent

Las señales RF de entrada y salida llegan al atenuador a través de conectores hembra de 3.5 mm (puesto que se trata del modelo Opt.004 del atenuador).

La hoja de características de este componente se adjunta en el Anexo D.- Hojas de características de los componentes.

2.4 Funcionalidad

Las señales de alimentación de 15 V y 5 V se conectan a filtros EMI para evitar que señales interferentes causen errores en el funcionamiento del circuito. La señal de 15 V resultante se proporciona como señal de salida para su conexión al pin 10 del conector DIP, correspondiente a la alimentación del atenuador programable; la señal de masa correspondiente se conecta al pin 3 del conector DIP.

Puesto que las señales de control (*Thru* y *Att*) de cada sección del atenuador deben tener siempre niveles distintos entre sí, se empleará un único bit de control para cada celda, y a partir de éste se generan las señales de control correspondientes.

Para el diseño del circuito eléctrico se han seguido las sugerencias del fabricante, cuya propuesta es la mostrada en la *Fig. 1*:

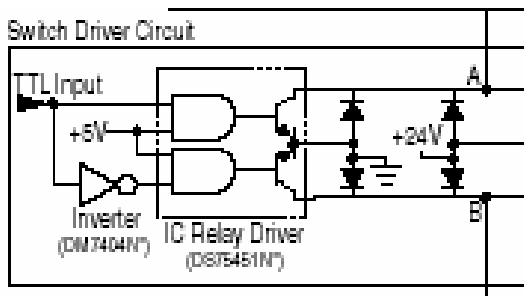

Fig. 1 - Circuito propuesto por el fabricante para la generación de las señales de control de cada una de las celdas del atenuador programable 84904K Opt015 Opt004 de Agilent

La señal de control TTL *CtlN* se niega mediante un inversor SN74LS04; de este modo se obtienen dos señales que tomarán en todo momento niveles distintos y que serán entrada del driver DS75452. Este driver realiza la conversión de estas señales a niveles de 0 y 15 V, necesarios para el control de las celdas, haciendo uso de diodos externos conectados a tierra y a la señal de alimentación de 15 V (no 24 V como aparece en la *Fig. 1*, puesto que se trata del modelo de atenuador Opt015).

Al circuito sugerido por el fabricante se han añadido resistencias de pull-up (*R4, R8, R12, R16*) para tener un nivel alto por defecto en cada señal de control *CtlN* de entrada, de modo que en ausencia de establecimiento de nivel de dicha señal, a la salida del driver los niveles generados son de 15 V para la señal *AttN*, y 0 V para la señal *ThruN*, y por lo tanto por defecto la celda correspondiente del atenuador no estará activada (no se atenuará la señal de RF).

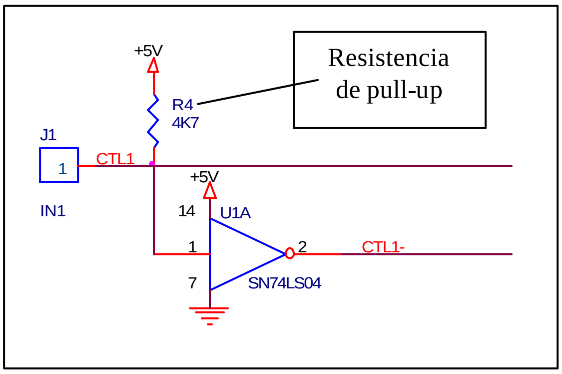

Fig. 2 – Resistencia de pull-up para cada señal de control procedente del bus de control

Se han incluido también resistencias de 1KΩ (*R3*, *R7*, *R11*, R15) entre la señal de alimentación de 5V y las entradas *A2*, *B1* del driver *DS75452*, para de este modo establecer constantemente un nivel alto TTL en estas entradas. La corriente máxima consumida por los terminales de entrada del driver es de 1mA (dato suministrado por el fabricante), lo que supondría una caída máxima de tensión en esta resistencia de 2V. En este caso límite, las entradas *A2* y *B1* presentarían una tensión de 3V, que está por encima del valor mínimo especificado para considerar un nivel alto TTL a la entrada del driver.

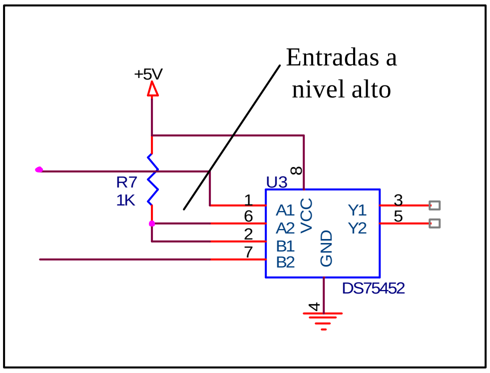

Fig. 3 – Resistencia para establecer nivel alto TTL en entradas del driver

Los valores de las salidas del driver en función del valor del bit de control de la celda se rigen por la siguiente tabla de verdad:

Bit de control	Valor TTL	Entradas del driver		Salidas del driver		Programación de la celda
CtlN	0	*A1*	0	*Y1* *(ThruN)*	15 V	*Atenúa*
		A2	1			
		B1	1	*Y2* *(AttN)*	0 V	
		B2	1			
	1	*A1*	1	*Y1* *(ThruN)*	0 V	*No atenúa*
		A2	1			
		B1	1	*Y2* *(AttN)*	15 V	
		B2	0			

Tabla 3 – Tabla de verdad del circuito diseñado

En la siguiente tabla se establecen las atenuaciones conseguidas con cada combinación de valores de los bits de control:

Bit de control	Valor TTL	Señales generadas por el driver	Atenuación programada en la celda
Ctl1	0	*Att1 = 0, Thru1 = 1*	*Celda 1 ? 1 dB*
	1	*Att1 = 1, Thru1 = 0*	*Celda 1 ? 0 dB*
Ctl2	0	*Att2 = 0, Thru2 = 1*	*Celda 2 ? 2 dB*
	1	*Att2 = 1, Thru2 = 0*	*Celda 2 ? 0 dB*
Ctl3	0	*Att3 = 0, Thru3 = 1*	*Celda 3 ? 4 dB*
	1	*Att3 = 1, Thru3 = 0*	*Celda 3 ? 0 dB*
Ctl4	0	*Att4 = 0, Thru4 = 1*	*Celda 4 ? 4 dB*
	1	*Att4 = 1, Thru4 = 0*	*Celda 4 ? 0 dB*

Tabla 4 – Atenuación programada por cada bit de control

Por otro lado, a la salida del driver se sitúan resistencias de 2K37O (*R1, R2, R5, R6, R9, R10, R13,* R14) entre la señal de alimentación de 15 V y los diodos, para protegerlos de una posible circulación de corriente excesiva.

En el caso de tener un nivel bajo a la salida, y suponiendo el caso peor, en el que la caída de tensión en la resistencia es máximo (15 V), la corriente que circulará por esa rama será de 6.4 mA, y la potencia disipada en las resistencias de 0.094 W (inferior a la potencia máxima especificada de 0.1 W).

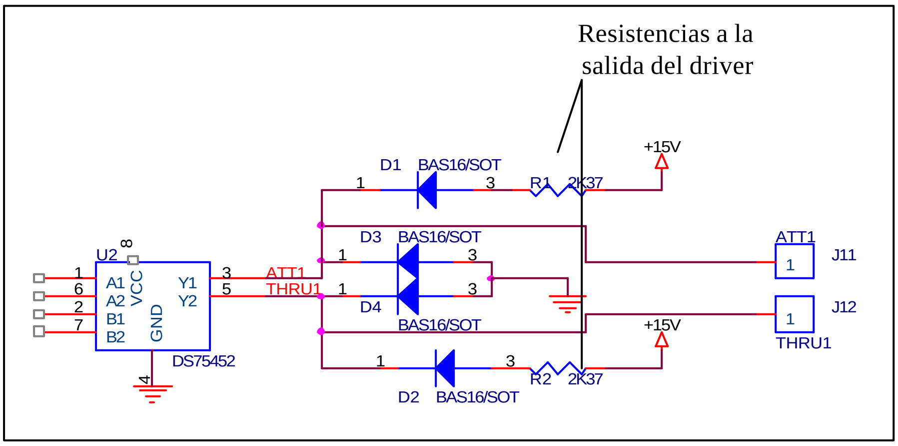

Fig. 4 – Resistencias de protección entre la señal de alimentación de 15V y los diodos

El circuito eléctrico empleado por lo tanto para el control de cada una de las celdas a partir del bit de control correspondiente es el siguiente:

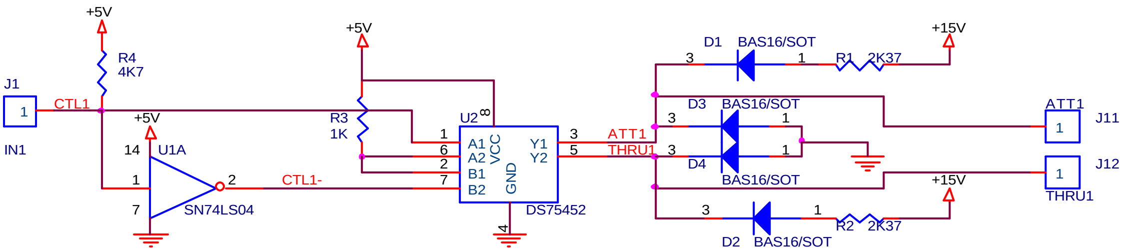

Fig. 5 - Circuito empleado para la generación de las señales de control de cada una de las celdas del atenuador programable 84904K Opt015 Opt004 de Agilent

En concreto, este circuito es el empleado para el control de la celda 1 del atenuador, siendo idéntico para el resto.

3 Construcción de la placa e inserción en el módulo

3.1 Placa de circuito impreso

El circuito de control descrito se ha fabricado en la fresadora LPKF del CAY, y se han soldado los componentes en ella.

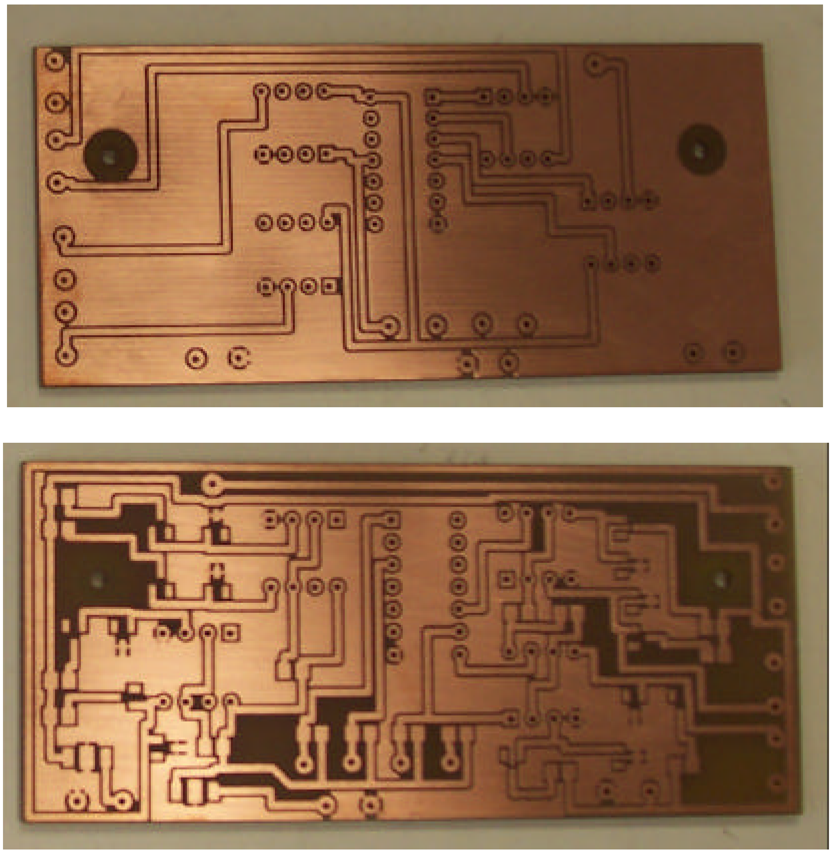

Fig. 6 - Caras frontal y trasera de la placa de circuito impreso para el control del atenuador programable, fabricada con la fresadora LPKF del CAY

Los diodos que aparecen en el diseño son BAS16, con encapsulado SOT23. Sin embargo, existía un fallo en la herramienta OrCAD; dicho fallo consistía en una numeración errónea de las patillas del componente, estando cátodo y ánodo intercambiados. Debido a esto, al exportar el diseño al programa CADStar, la huella de los diodos aparecía en orientación invertida; esto obligó a reemplazarlos por diodos 1N4148, que pudieron soldarse en la posición adecuada.

Este error del componente BAS16 de la librería "Discrete" del programa OrCAD ha sido corregido; en la Fig. 7 se muestra la numeración de patillas correcta.

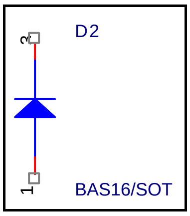

Fig. 7 – Modelo OrCAD del diodo SMD BAS16, con numeración de pines corregida

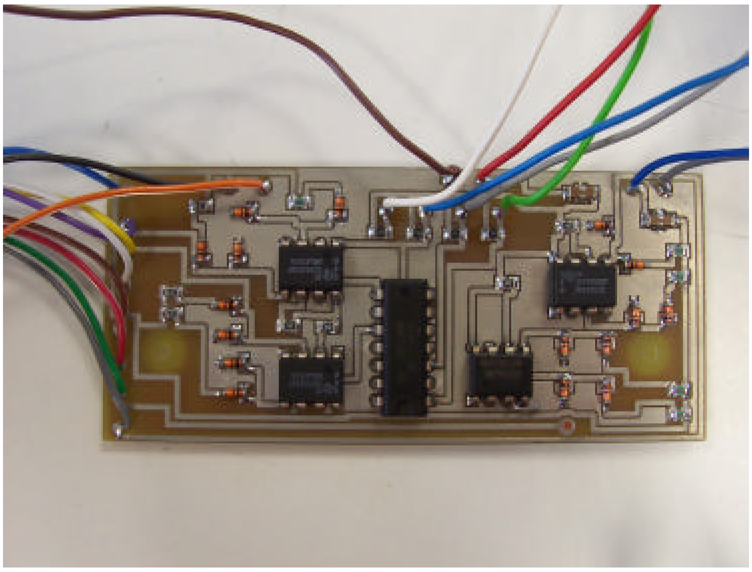

Fig. 8 – Placa de circuito impreso para el control del atenuador programable, con componentes soldados

3.2 Inserción en el submódulo de ruido

La placa realizada se ha integrado en el submódulo de ruido del receptor de 22 GHz, atornillada sobre el atenuador 84904K de Agilent aprovechando los orificios que éste presenta en su superficie.

La conexión de las entradas al bus de control y alimentación sigue la correspondencia descrita en la siguiente tabla:

Conector en la placa	Señal de entrada	Conexión en el módulo
J1	*IN1*	Pin 4c bus de control NM_VAR_ATT_D0
J2	*IN2*	Pin 5c bus de control NM_VAR_ATT_D1
J3	*IN3*	Pin 6c bus de control NM_VAR_ATT_D2
J4	*IN4*	Pin 7c bus de control

		NM_VAR_ATT_D3
J5V	*5V y GND*	Pin 1c bus de control (5V) Pin 32c bus de control (GND)
J15V	*15V y GND*	Pin 1a bus de control (15V)

Tabla 5 – Conexión de las entradas a la placa en el submódulo de ruido

El pin de GND del conector de alimentación de 15V no necesita ser conectado al bus de alimentación, puesto que existe un cortocircuito entre las masas de ambos conectores de alimentación (5 V y 15 V) a través del plano de masa de la placa. Por lo tanto, tan sólo uno de los pines de GND de dichos conectores deberá conectarse al pin correspondiente del bus de alimentación del receptor; se ha escogido conectar el pin de GND del conector de alimentación de 5 V.

Las salidas del circuito se conectan al atenuador programable 84904 de Agilent siguiendo la correspondencia descrita en la siguiente tabla:

Conector en la placa	**Señal de salida**	**Conexión al atenuador**	
		Pin del conector DIP	**Color**
J11	*Thru1*	1	Marrón
J12	*Att1*	2	Rojo
J21	*Thru2*	5	Verde
J22	*Att2*	8	Gris
J31	*Thru3*	4	Amarillo
J32	*Att3*	9	Blanco
J41	*Thru4*	6	Azul
J42	*Att4*	7	Violeta
J015V	*15V*	10	Negro
$J015V_{GND}$	*GND*	3	Naranja

Tabla 6 – Conexión de las salidas de la placa al atenuador 84904 de Agilent

4 Pruebas realizadas

Las señales de alimentación de 5 V y 15 V se han generado mediante la fuente HP E3631A, y se han conectado junto a las señales de masa a las entradas correspondientes de la placa de circuito impreso (*J15V, J5V*).

La salida de alimentación de la placa (*J015V*), con señales de 15 V y de masa, se ha conectado a los cables de alimentación del atenuador programable (pines 10 y 3 del conector DIP).

Se ha realizado la conexión de los pines de salida de la placa a los pines correspondientes del conector DIP del atenuador, según la correspondencia detallada en la Tabla 6.

Las señales de entrada de la placa son TTL, por lo que las entradas se conectarán a las señales de 5 V y masa generadas para la alimentación, de forma alternativa dependiendo de si se desea un 1 ó un 0 lógico.

Se ha comprobado que el circuito cumple las especificaciones descritas en la Tabla 4. Para cada valor posible de los bits de control, las salidas toman los valores adecuados, y el atenuador presenta la atenuación programada.

En ausencia de señal de entrada, las resistencias de pull-up fuerzan un 1 lógico. El nivel de la señal medida en este caso es de 4.93 V, lo que implica que por dichas resistencias circula una corriente de unos 15 µA. Este nivel de señal de entrada es suficiente para ser interpretada como un 1 lógico por los circuitos integrados a los que está conectada (driver e inversor).

Dos de las entradas de cada driver están conectadas a la tensión de 5 V a través de una resistencia de 1 kO. La tensión medida en estas entradas es también de 4.94 V, por lo que la corriente que circula por estas resistencias es de unos 60 µA.

Cuando las señales de entrada se encuentran a nivel alto, la corriente suministrada por la fuente de alimentación de 5 V es de 121 mA. Ésta se debe a:

- Consumo de las entradas del inversor (CI SN74LS04).
  Puede considerarse despreciable. El fabricante especifica una corriente de entrada de 0.1 mA en el caso de que dicho pin presente una tensión de 7 V. La tensión que presentan las entradas del inversor es de 4.93 V, por lo que la corriente consumida será aún menor.

- Consumo de las entradas del driver (CI DS75452).
  Puede considerarse despreciable. El fabricante especifica una corriente máxima de 1 mA en el caso de que la entrada se encuentre a una tensión máxima de 5.5 V, y de 40µA si la tensión de entrada es de 2.7 V.

Sabemos que la corriente que circula por cada una de las resistencias de pull-up es de 15 µA, y comprende una de las entradas del driver correspondiente y una de las entradas del inversor. En esta placa se incluyen 4 resistencias de este tipo, por lo que en total estas corrientes suman 60 µA.
Dos de las entradas de cada driver se encuentran conectadas a la fuente de 5 V a través de una resistencia de 1 KO, por la que se sabe que la corriente es de 60 µA; esto significa que cada entrada consume una corriente de 30 µA. Puesto que se tienen 4 drivers, en total estas entradas supondrán un consumo de 240 µA.

El consumo conjunto que las entradas de driver e inversor suponen a la fuente de alimentación de 5 V sería de unos 300 µA; de este modo se constata que es un valor despreciable frente al consumo total de 121 mA.

- Consumo del inversor (CI SN74LS04).

  El fabricante especifica una corriente consumida por el circuito integrado, en el caso de que todas las entradas se encuentren a nivel alto, de 3.6 mA como valor típico y 6.6 mA como valor máximo. En el caso actual, 4 de las 6 entradas se encuentran a nivel alto, por lo que se puede considerar un consumo máximo de unos 5 mA.

- Consumo del driver (CI DS75452).

  El fabricante suministra una especificación para el caso de tener ambas salidas a un mismo nivel: a nivel alto 11 mA como valor típico y 14 mA como nivel máximo, y a nivel bajo 56 mA como valor típico y 71 mA como valor máximo. En nuestro caso, ambas salidas tendrán siempre un nivel opuesto, por lo que se podría considerar un valor intermedio entre ambos.
  Tras los cálculos de consumo realizados, se puede concluir que la mayor parte de la corriente suministrada está destinada a la alimentación de los drivers del circuito. Se puede considerar que para este fin se emplean al menos 115 mA de los 121 mA totales; esto es, cada uno de los 4 drivers incluidos en el circuito consume menos de 29 mA de corriente.

Cuando las señales de entrada se encuentran a nivel bajo, el consumo aumenta unos 3 mA, debido a los siguientes efectos:

- La corriente que circula por las resistencias de pull-up será mayor, puesto que al tener en ellas una caída de tensión de prácticamente 5V, la corriente que circule será de más de 1 mA. Esto supondría un aumento en la corriente requerida de unos 4 mA.

- Por otro lado, el consumo del inversor será menor, puesto que 4 de las 6 entradas se encontrarán a nivel bajo. El fabricante especifica un consumo en el caso de que todas las entradas se encuentren a nivel bajo de 1.2 mA como valor típico y 2.4 mA como valor máximo. Esto supone una reducción en el aumento de la corriente requerida, resultando de 3 mA en lugar de 4 mA.

Por otro lado, la corriente suministrada por la fuente de alimentación de 15 V para el funcionamiento del circuito es de 24 mA (incluyendo el atenuador programable, al que se encuentra conectado).

El consumo de la fuente de 15 V aumenta significativamente cuando se produce la conmutación de las celdas del atenuador, al variar la atenuación programada.

Este pico de corriente es de unos 70 mA para cada celda, al conmutar el bit de control de 0 a 1 (esto es, al desactivar la celda), y algo mayor, unos 80 mA, para activar la celda, al conmutar el bit de control correspondiente de 1 a 0.

El pico de corriente total necesario para conmutar todas las celdas al mismo tiempo es de unos 270 mA.

Anexo A.- Esquema del submódulo de ruido

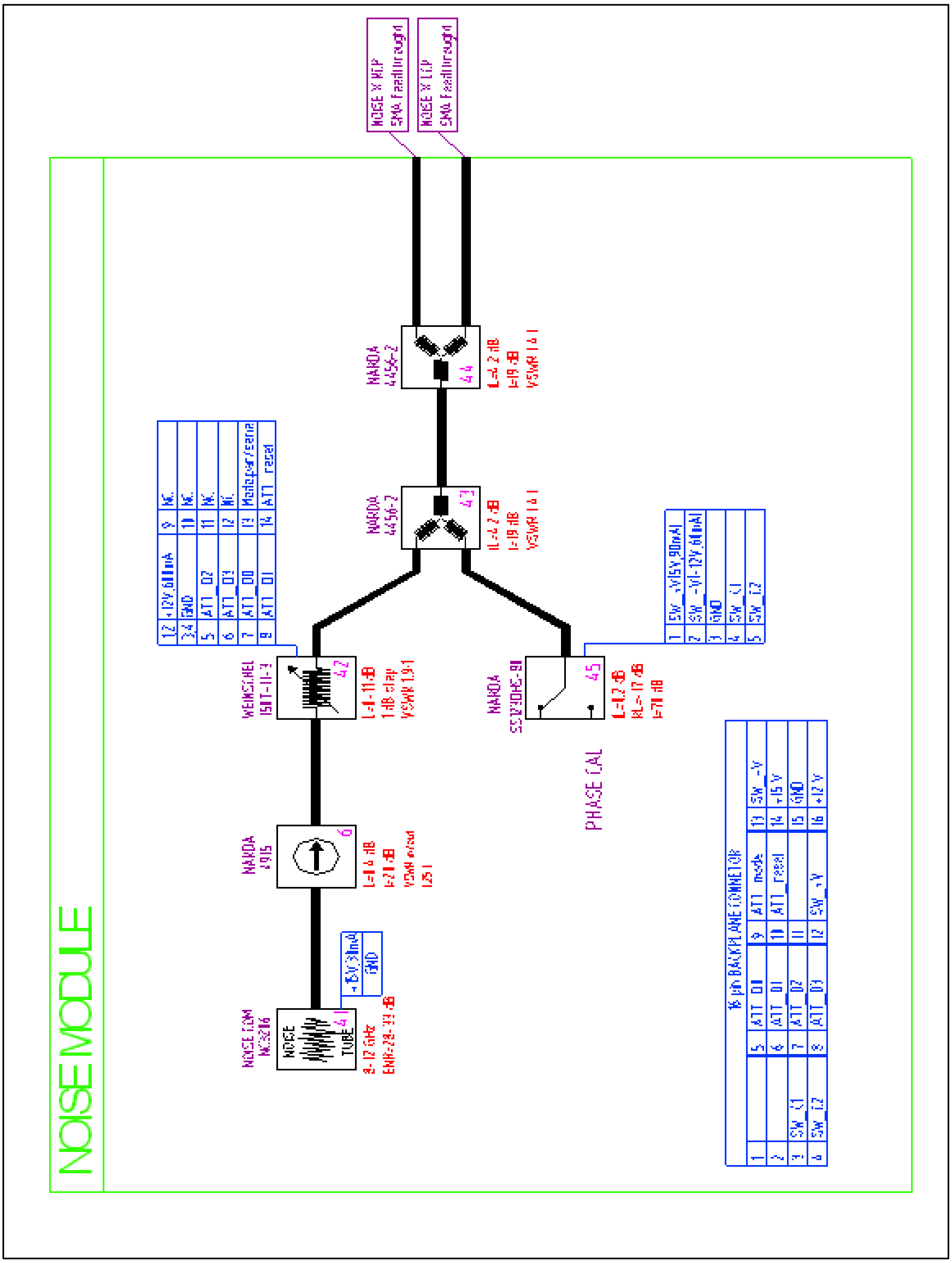

Figura 1. Esquema del submódulo de ruido; las señales de control generadas por la placa de control van destinadas a el atenuador programable (elemento 42)

Anexo B.- Esquema eléctrico del circuito

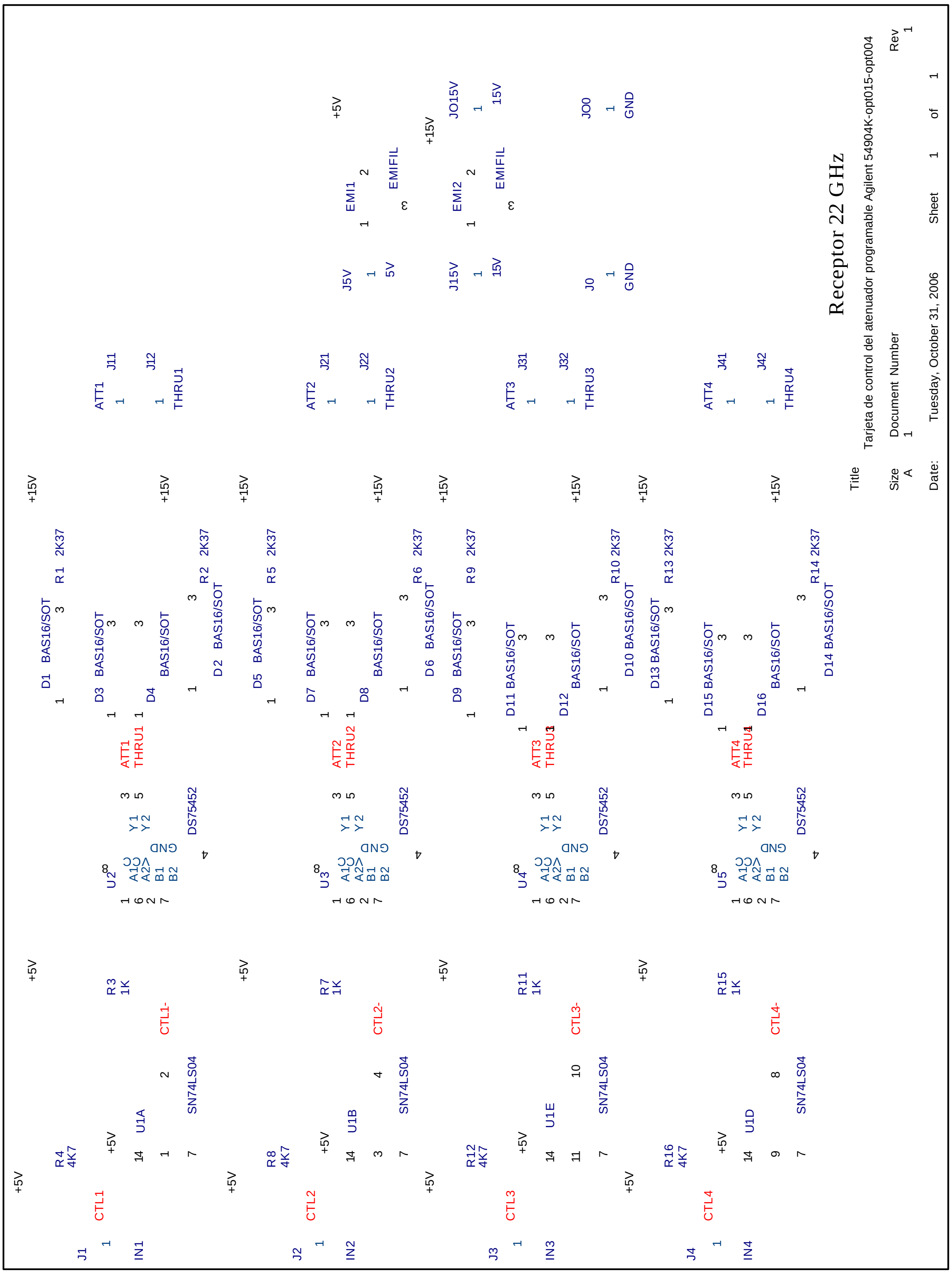

Figura 2. Esquema eléctrico de la placa de control del atenuador programable del submódulo de ruido

Anexo C.- Layout de la placa

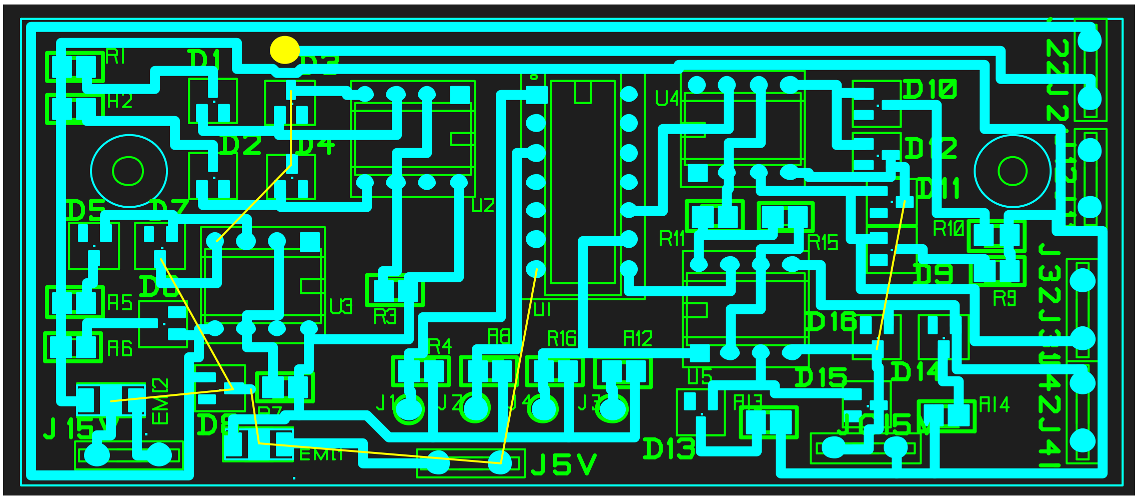

Figura 3. Layout de la cara superior de la placa de control del atenuador programable del submódulo de ruido (sin planos de masa)

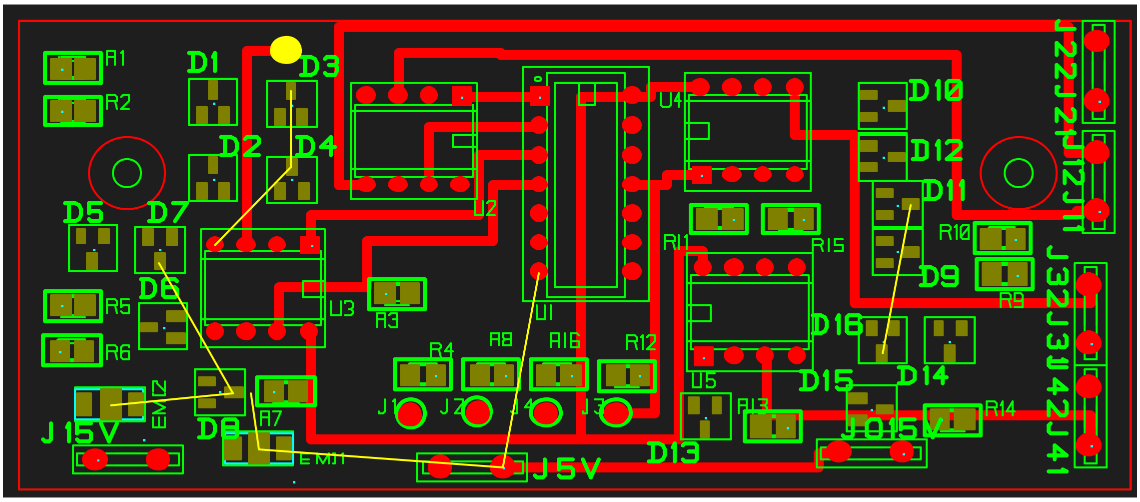

Figura 4. Layout de la cara inferior de la placa de control del atenuador programable del submódulo de ruido (sin planos de masa)

Anexo D.- Hojas de características de los componentes

Agilent 84904, 6, 7K/L
Programmable Step Attenuators

Data Sheet

Excellent repeatability
High accuracy
Excellent reliability, long life

Features and description

- DC to 26.5 GHz, DC to 40 GHz frequency coverage
- Optional calibration data
- 0 to 11 dB, 70 dB, 90 dB
- 1 dB steps, 10 dB steps
- Excellent repeatability
- High accuracy
- Excellent reliability, long life
- Exceptionally low insertion loss

These attenuators offer repeatability of better than 0.03 dB and excellent life (greater than 5 million switching cycles per section).

This family of programmable step attenuators offers coaxial measurements to 26.5 GHz (K models) or to 40 GHz (L models), in a compact, rugged design. The first model in this family is the Agilent Technologies 84906K/L, which offers outstanding performance with an attenuation range of 0 to 90 dB in 10 dB steps. Other models include the Agilent 84904K/L, with 0 to 11 dB of attenuation in 1 dB steps, and the Agilent 84907K/L, with 0 to 70 dB of attenuation in 10 dB steps.

This latest design evolution sets new standards for size and performance. High attenuation accuracy and low SWR are achieved through the use of miniature thin-film attenuation cards composed of high-stability tantalum nitride film on a sapphire substrate. Insertion loss performance is outstanding, with less than 2 dB of loss at 26.5 GHz and only 2.4 dB at 40 GHz (figure 1). The compact size of the units, 35% smaller than the 8495/7 (26.5 GHz) family, allows for easy integration into instruments and ATE systems.

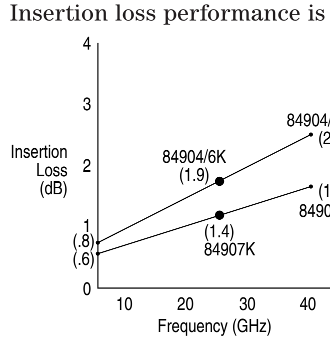

Figure 1. Insertion loss

This family of step attenuators offers three connector types. For operation to 40 GHz, the 84904/6/7L models offer either the 2.4 mm connector, which is recommended for top performance and for rugged and repeatable connections, or the 2.92 mm connector, which is compatible with SMA and 3.5 mm connectors but is more delicate. For operation to 26.5 GHz, the 84904/6/7K models offer the 3.5 mm connector. This connector is compatible with SMA and 2.92 connectors, but is more rugged. Each model in the 84904/6/7K and L family comes with two female connectors (standard) or may be ordered with one female and one male connector for easy insertion into a microwave chain or to combine the 1 dB step

Agilent Technologies

84904 with a 10 dB step 84906 or 84907 to cover an attenuation range of 121 dB or 81 dB in 1 dB steps.

Individual calibration data reports of attenuation and SWR are available. This data, measured with an Agilent automatic network analyzer, can be ordered as Option 8490XX-UK6.

Attenuation switching and control

These units feature the same small solenoids and switching circuits as the Agilent Technologies 8494/5/6/7 step attenuator family. Switching time is a maximum of 20 milli-seconds, including contact settling time. Once switched, the units are latched with permanent magnets, capable of withstanding shocks over 10 Gs. The solenoids automatically disconnect after switching, which minimizes the attenuators' power requirements and simplifies the driver circuit design (figure 3). Solenoids are available in either 24 volt (standard, Option 8490xx-024), 15 volt (Option 8490xx-015), and 5 volt (Option 8490xx-011) ranges to fit your instrument or system requirements.

The units come equipped with 10-pin DIP headers for connecting dc control lines. Available accessories include a 203 mm (8 inch) or 406 mm (16 inch) ribbon cable with DIP-type connectors that is compatible with standard 14-pin DIP IC sockets (11764-60002 or 11764-60003, respectively). Alternatively, a 1524 mm (5 foot) cable with free wires for direct soldering (11764-60001), or a 1524 mm (5 foot) drive cable that connects to the 11713A attenuator/ switch driver, allowing for easy integration into GPIB-controlled automatic test systems (11764-60004), may be ordered.

Selection switching

Figure 2 shows one attenuator section schematic. Each section utilizes one solenoid with dual coil windings, one coil to switch in the attenuator card (e.g. 10 dB) and one coil to switch in the thru line (0 dB).

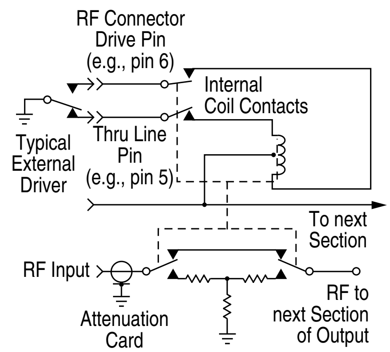

Figure 2. Section electrical diagram

With positive voltage applied to the common pin, the state (attenuator card or thru line) of a particular section is determined by connecting its attenuator card pin or thru pin to a negative voltage or ground. Figure 4 defines the pin assignments and wire color code for the 11764-60001/60002/60003 drive cables. Table 1 is a solenoid drive pin and attenuation guide. Table 2 (on page 4) defines recommended attenuator section activation.

As a section is switched, the internal contacts of the activated coil open, thus shutting off current flow. At the same time, the internal contacts for the other coil close so that it can be activated when desired. Figure 3 shows a section that has been switched to the attenuator card position (note the closed thru line coil contact). The switching is "break-before-make" type, thus a momentary interruption of the RF signal occurs at switching.

Although all sections can be switched simultaneously, the attenuator driver must not allow both pins of the same section (e.g. Section 1, pins 1 and 2) to be activated concurrently, or else that section would cycle rapidly. All terminals are "floating," so bipolar or unipolar power supplies can be used.

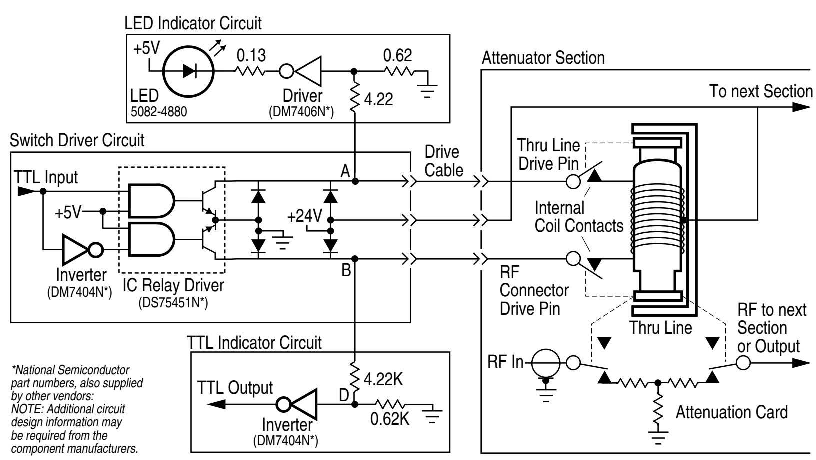

Figure 3. Driver and indicator circuits for one section of an Agilent 84904, 6, 7 K/L

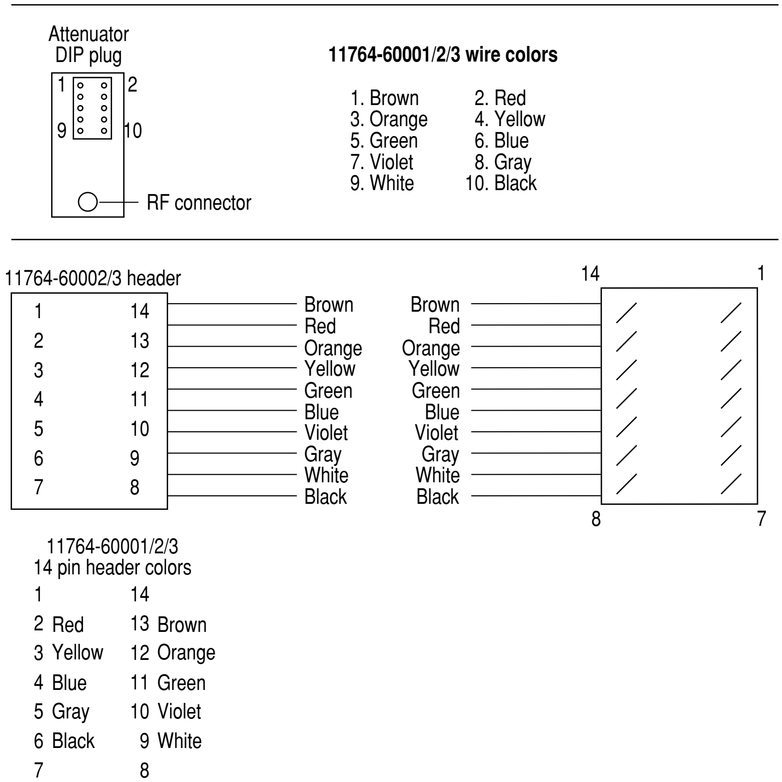

Figure 4. Attenuator switching pinout

Table 1. Solenoid pin and attenuation guide

Section:	Section 1		Section 2		Section3		Section 4	
Model Number	**Thru Line**	**Attn Card**	**Thru Line**	**Attn Card**	**Thru Line**	**Attn Card**	**Thru Line**	**Attn Card**
84906K/L								
Attenuation (dB)	0	10	0	20	0	30	0	30
Actuating pin	1	2	5	8	4	9	6	7
11764-60004 plug								
Pin number	5	6	7	8	9	10	11	12
11764-60002/60003 flat								
Header pin number	13	2	11	5	3	9	4	10
84907K/L								
Attenuation (dB)	0	10	0	20	0	40		
Actuating pin	1	2	5	8	4	9		
11764-60004 plug								
Pin number	5	6	7	8	9	10		
11764-60002/60003 flat								
Header pin number	13	2	11	5	3	9		
84904K/L								
Attenuation (dB)	0	1	0	2	0	4	0	4
Actuating pin	1	2	5	8	4	9	6	7
11764-60004 plug								
Pin number	5	6	7	8	9	10	11	12
11764-60002/60003 flat								
Header pin number	13	2	11	5	3	9	4	10

Pin 10 is +V Supply

Typical driver circuit

Figure 3 shows an economical TTL compatibility driver circuit for a single attenuation section which utilizes and IC relay driver and an inverter. A TTL “HI” input to the driver switches in the attenuation card, while a “LO” will activate the thru line for that section. This provides a complimentary driver for the section which assures that only one solenoid of the pair is activated at a time. Diode protection is required to protect the IC from the solenoid voltage flyback.

Switch position can be indicated remotely by utilizing the open and closed states of the internal coil contacts. Connected at A and B in figure 3 are two indicator circuits, one providing a TTL output and one that activates an LED. These circuits will output a TTL “HI (LED lamp ON”) if the attenuation card is in the RF circuit, and will output a TTL “LO” (LED lamp “OFF”) if the thru line is in the RF circuit. Since current is drawn through the coil for these circuits, inadvertent switching is prevented by limiting the current to 5 mA.

Agilent Technologies assumes no responsibility for the use of any circuits described herein and makes no representation or warranties, express or implied, that such circuits are free from patent infringement.

Drive cables

11764-60001	10 pin DIP to 60″ long ribbon cable
11764-60002	10 pin DIP to 14 pin DIP, 8″ long
11764-60003	10 pin DIP to 14 pin DIP, 16″ long
11764-60004	10 pin DIP to 12 pin Viking connector, 60″ long. Used with 11713A driver
11764-60006	10 pin DIP to (4) 4 pin BERG connectors, 30″ long. Used with 87130A or 70611A driver

Table 2. Attenuator section activation guide

Recommended switching sequence: The following switching sequence (ie. which 30 dB section to use for the 84906K/L or which 4 dB section for the 84904K/L should be followed to insure performance to specs.

Attenuation selected

84906K/L	**0 dB**	**10 dB**	**20 dB**	**30 dB**	**40 dB**	**50 dB**	**60 dB**	**70 dB**	**80 dB**	**90 dB**
Section 1 (10 dB)		X			X			X		X
Section 2 (20 dB)			X			X			X	X
Section 3 (30 dB)				X	X	X	X	X	X	X
Section 4 (30 dB)							X	X	X	X

84907K/L	**0 dB**	**10 dB**	**20 dB**	**30 dB**	**40 dB**	**50 dB**	**60 dB**	**70 dB**
Section 1 (10 dB)		X		X		X		X
Section 2 (20 dB)			X	X			X	X
Section 3 (40 dB)					X	X	X	X

84904K/L	**0 dB**	**1 dB**	**2 dB**	**3 dB**	**4 dB**	**5 dB**	**6 dB**	**7 dB**	**8 dB**	**9 dB**	**10 dB**	**11 dB**
Section 1 (1 dB)		X		X		X		X		X		X
Section 2 (2 dB)			X	X			X	X			X	X
Section 3 (4 dB)					X	X	X	X	X	X	X	X
Section 4 (4 dB)									X	X	X	X

Switching notes: Pins relate to 10-pin attenuator header as shown (Table 1), NOT terminating connector on any attached drive cable. Solenoids are magnetic latching type; drive voltage may be removed after switching. Current is self-interrupting in less than 20 ms.

GPIB attenuator/switch driver

Employing programmable step attenuators and switches in an automatic test system becomes an easy task when the Agilent 11713A attenuator/switch driver is specified into the system.

The 11713A has all of the necessary features to provide GPIB control of up to two programmable attenuators of the 84904/6/7 series, and concurrently up to two electro-mechanical switches (e.g., the 8671B or 8762 Series).

The 11713A includes an integral power supply (with short circuit protection) that can simultaneously provide 125 millamps at 24 volts to all contacts for control of the attenuators and switches, so no external power supply is needed. Connecting between the 11713A and the 84904/6/7 step attenuators is easy with the 11764-60004 drive cable.

The 11713A also features convenient front panel keys so the user can manually activate the individual attenuation sections and switches when in the "local" mode. Switching time for the drivers is less than 10 milliseconds.

Optional calibration data for the Agilent 84904/6/7

Use of calibration data (i.e., accuracy, recorded, data of a device's characteristics) has always been an effective means of reducing measurement uncertainty at RF and microwave frequencies. Step attenuators have long been used as reference standards in the measurement of gain, attenuation, and receiver sensitivity. Since the accuracy specifications include margins for frequency response and unit-to-unit variations, calibration data can improve overall measurement uncertainty.

Calibration data is available as Option 8490xx-UK6 and is generated from measurements made by an Agilent network analyzer.

Option 8490xx-UK6 provides a tabular list of attenuation and reflection coefficients in 250 MHz steps from 1500 MHz to 40 GHz. Measurements are traceable to NIST (National Institute of Standards and Technology, formerly NBS) standards and feature very low measurement uncertainties (See tables 3 and 4).

For devices with option 8490xx-006 and option 8490xx-106, option 8490xx-UK6 and NIST traceability are not available.

Table 3. Agilent 84904/6/7K/L reflection coefficient data uncertainty

Frequency Range (GHz)	
dc to 12.4	± .017
14.4 to 26.5	± .023
26.5 to 34	± .025
34 to 40	± .028

Table 4. Agilent 84904/6/7K/L attenuation data uncertainties

Attenuation (dB)	dc to 20 GHz	20 to 26.5 GHz	26.5 to 40 GHz
0	± 0.12	± 0.12	± 0.15
10	± 0.16	± 0.24	± 0.30
20	± 0.16	± 0.25	± 0.30
30	± 0.17	± 0.30	± 0.30
40	± 0.32	± 0.47	± 0.30
50	± 0.36	± 0.54	± 0.30
60	± 0.36	± 0.54	± 0.30
70	± 0.52	± 0.72	± 0.35
80	± 0.50	± 0.52	± 0.60
90	± 0.66	± 0.91	± 1.05

Attenuator setting

Attenuation accuracy (±dB; referenced from 0 dB setting):

	84907K/L										
	84906K/L										
Attenuator setting	10	20	30	40	50	60	70	80	90		
Frequency range dc to 40 GHz[2]	0.5	0.6	0.7	1.0	1.2	1.6	1.8	2.7	2.9		
	84904K/L										
Attenuator setting (dB)	1	2	3	4	5	6	7	8	9	10	11
Frequency range											
dc to 18 GHz	0.35	0.45	0.55	0.55	0.55	0.55	0.60	0.60	0.65	0.70	0.80
18 to 26.5 GHz	0.40	0.50	0.70	0.70	0.70	0.70	0.80	0.80	0.85	0.90	1.10
26.5 to 40 GHz[2]	0.60	0.60	0.80	0.80	0.80	0.90	1.10	1.10	1.20	1.30	1.50

1 Step-to-step accuracy is the maximum variation from the nominal step size when changing attenuation values. It is a second specification on accuracy, and is used in combination with the absolute accuracy specifications to limit maximum allowable variation from nominal. Typical step-to-step accuracy for the 84906L and 84907L is ±0.6 dB to 26.5 GHz, ±0.9 dB to 40 GHz; for the 84904L is ±0.3 to 26.5 GHz, ±0.4 to 40 GHz.

2 Attenuation accuracy to 26.5 GHz for K models.

Specifications

Insertion loss

(in dB 0 dB position, f = freq. in GHz)

84904K/L	(0.8 + 0.04xf)
84906K/L	(0.8 + 0.04xf)
84907K/L	(0.6 + 0.03xf)

SWR	Connector Option	dc to 12.4 GHz	12.4 GHz to 34 GHz	34 GHz to 40 GHz
L models				
84904L	with 101	1.3	1.7	1.8
84904L	with 006	1.5	1.9	2.0
84904L	with 100	1.3	1.7	1.8
84904L	with 106	1.5	1.9	2.0
84906L	with 101	1.3	1.7	1.8
84906L	with 006	1.5	1.9	2.0
84906L	with 100	1.3	1.7	1.8
84906L	with 106	1.5	1.9	2.0
84907L	with 101	1.25	1.5	1.7
84907L	with 006	1.4	1.7	1.9
84907L	with 100	1.25	1.5	1.7
84907L	with 106	1.4	1.7	1.9

SWR	Connector Option	dc to 12.4 GHz	12.4 GHz to 26.5 GHz
K models			
84904K	004	1.3	1.7
84904K	104	1.3	1.7
84906K	004	1.3	1.7
84906K	104	1.3	1.7
84907K	004	1.25	1.5
84907K	004	1.25	1.5

Attenuation temperature coefficient
Less that 0.0001 dB/dB/C°

Power sensitivity
0.001 dB/Watt

RF Input power (max.)
1 Watt average, 50 Watts peak (10 µs max. pulse width)

Life (min.)
5 million cycles per section

Repeatibility
0.03 dB, typical

Environmental capabilities
(Up to 5 million cycles)

Temperature, operating
–20°C to +75°C

Temperature, non-operating
–55°C to +85°C

Altitude, operating
4,570 meters (15,000 ft.)

Altitude, non-operating
13,700 meters (50,000 ft.)

Humidity
Cycling 5 days, 40°C at 95% RH with condensation

Shock operating
10 Gs, six ms, on six sides, three blows

Shock, non-operating
500 Gs, 1.8 ms, in six directions

Vibration, operating
5 Gs, 34-2000 Hz

EMC
Radiated interference is within the requirements of MIL-STD-461 method RE02, VDE 0871 and CISPR Publication II

Mechanical information

Net weight	84904K/L	84906K/L	84907K/L
	291 grams (10.3 oz)	291 grams (10.3 oz)	229 grams (8.1 oz)

Mounting position (any)

RF connectors

2.4 mm connectors standard, L models only
2.92 mm (SMA compatible), L models only
3.5 mm (SMA compatible), K models only

Switching speed

Maximum 20 msec including settling time

Solenoids	Coil voltage	Switching Current[1]	Nominal coil impedance
Option 024	24 V (20 to 30 V)	125 mA (at 24 V)	190 Ω
Option 015	15 V (13 to 22 V)	188 mA (at 15 V)	80 Ω
Option 011	5 V (4.5 to 7 V)	325 mA (at 5 V)	17 Ω

1 Current per section; approximately 10 msec duration before internal contacts open the coil circuit

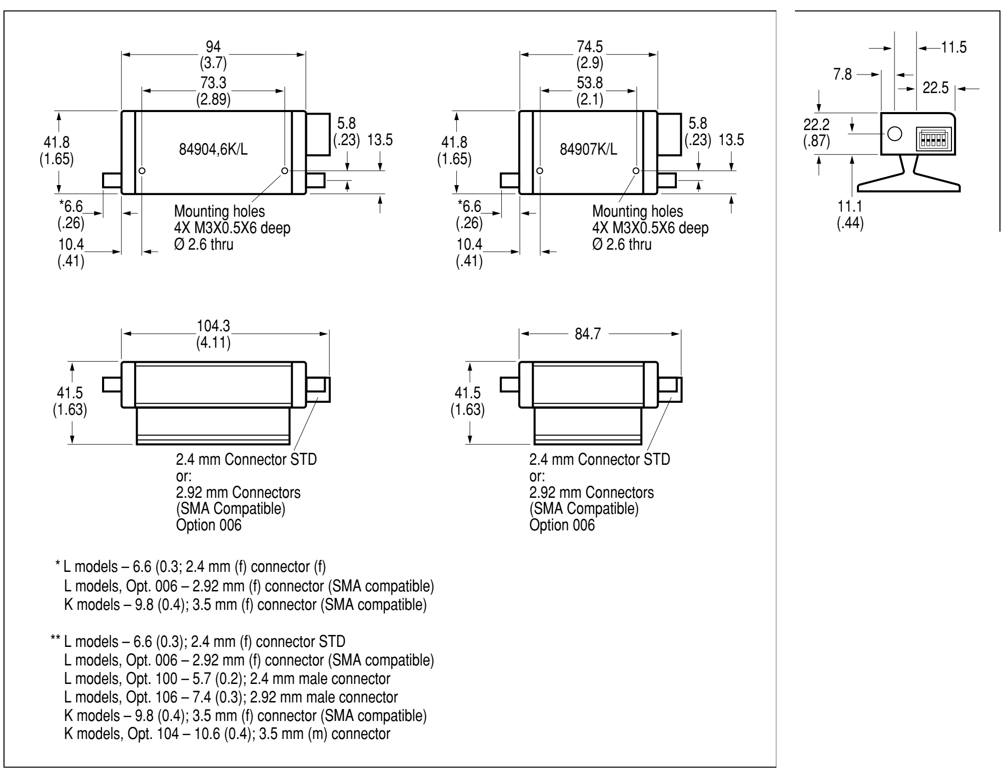

Figure 5. Dimensions are in millimeters and inches.

Ordering information

Programmable step attenuators

84904K 0 to 11 dB, 1 dB steps; dc to 26.5 GHz

84904L 0 to 11 dB, 1 dB steps; dc to 40.0 GHz

84906K 0 to 90 dB, 10 dB steps; dc to 26.5 GHz

84906L 0 to 90 dB, 10 dB steps; dc to 40.0 GHz

84907K 0 to 70 dB, 10 dB steps; dc to 26.5 GHz

84907L 0 to 70 dB, 10 dB steps; dc to 40.0 GHz

Options

To add options to a product, use the following ordering scheme:

Model: 84904/6/7x (x = K, L)

Model options: 84904/6/7x-opt#1 or 84904/6/7x-opt#2

Supply voltage (must choose one)

84904/6/7x-011 5 V dc supply voltage

84904/6/7x-015 15 V dc supply voltage

84904/6/7x-024 24 V dc supply voltage (standard option)

RF connectors (must choose one)

84904/6/7K-004 • 3.5 mm female connector, 3.5 mm female connector (standard option)

84904/6/7K-104 • 3.5 mm male connector, 3.5 mm female connector

84904/6/7L-006 • 2.92 mm female connector, 2.92 mm female connector (UK6 not available with this option)

84904/6/7L-100 • 2.4 mm male connector, 2.4 mm female connector

84904/6/7L-101 • 2.4 mm female connector, 2.4 female connector (standard option)

84904/6/7L-106 • 2.92 mm male connector, 2.92 mm female connector (UK6 not available with this option)

Calibration documentation (optional)

84904/6/7x-UK6 Calibration data

Accessories (optional)

11764-60001 • 10-pin dip plug (for attenutor connection) to 1524 mm (5 foot) ribbon cable

11764-60002 • 203 mm (8 inch) ribbon cable with 14-pin headers, female 10-pin receptacle

11764-60003 • 406 mm (16 inch) ribbon cable with 14-pin headers, female 10-pin receptacle

11764-60004 • Interconnect cable 10-pin dip plug to "Viking" connector (for use with 11713A)

Phone or Fax

United States:
(tel) 800 829 4444
(fax) 800 829 4433
Canada:
(tel) 877 894 4414
(fax) 800 746 4866
China:
(tel) 800 810 0189
(fax) 800 820 2816
Europe:
(tel) 31 20 547 2111
Japan:
(tel) (81) 426 56 7832
(fax) (81) 426 56 7840

Korea:
(tel) (080) 769 0800
(fax) (080)769 0900
Latin America:
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www.agilent.com/find/contactus

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5963-6944E

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BAS16

SURFACE MOUNT FAST SWITCHING DIODE

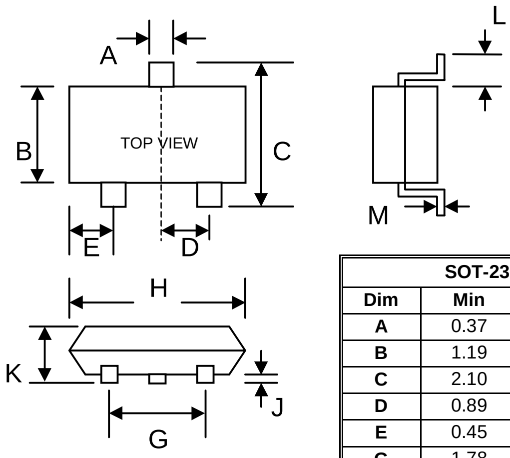
WTE
POWER SEMICONDUCTORS

Features

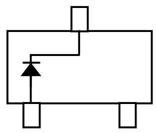
- High Conductance
- Fast Switching
- Surface Mount Package Ideally Suited for Automatic Insertion
- For General Purpose and Switching
- Plastic Material – UL Recognition Flammability Classification 94V-O

Mechanical Data

- Case: SOT-23, Molded Plastic
- Terminals: Plated Leads Solderable per MIL-STD-202, Method 208
- Polarity: See Diagram
- Weight: 0.008 grams (approx.)
- Mounting Position: Any
- Marking: A6



TOP VIEW



SOT-23		
Dim	**Min**	**Max**
A	0.37	0.51
B	1.19	1.40
C	2.10	2.50
D	0.89	1.05
E	0.45	0.61
G	1.78	2.05
H	2.65	3.05
J	0.013	0.15
K	0.89	1.10
L	0.45	0.61
M	0.076	0.178
All Dimensions in mm		

Maximum Ratings @T_A=25°C unless otherwise specified

Characteristic	Symbol	Value	Unit
Non-Repetitive Peak Reverse Voltage	V_{RM}	100	V
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	75	V
Forward Continuous Current (Note 1)	I_F	300	mA
Average Rectified Output Current (Note 1)	I_O	200	mA
Peak Forward Surge Current (Note 1) @ t < 1.0µs	I_{FSM}	2.0	A
Power Dissipation (Note 1)	P_d	350	mW
Typical Thermal Resistance, Junction to Ambient Air (Note 1)	$R_{\theta JA}$	357	°C/W
Operating and Storage Temperature Range	T_j, T_{STG}	-65 to +150	°C

Electrical Characteristics @T_A=25°C unless otherwise specified

Characteristic	Symbol	Min	Max	Unit	Test Condition
Reverse Breakdown Voltage	$V_{(BR)R}$	75	—	V	@ I_{RS} = 100µA
Forward Voltage	V_F	—	0.855	V	@ I_F = 10mA
Reverse Leakage Current	I_R	—	1.0	µA	@ V_R = 75V
Junction Capacitance	C_j	—	2.0	pF	V_R = 0V, f = 1.0MHz
Reverse Recovery Time	t_{rr}	—	6.0	nS	$I_F = I_R$ = 10mA, I_{RR} = 0.1 x I_R, R_L = 100Ω

Note: 1. Device mounted on fiberglass substrate 40 x 40 x 1.5mm.

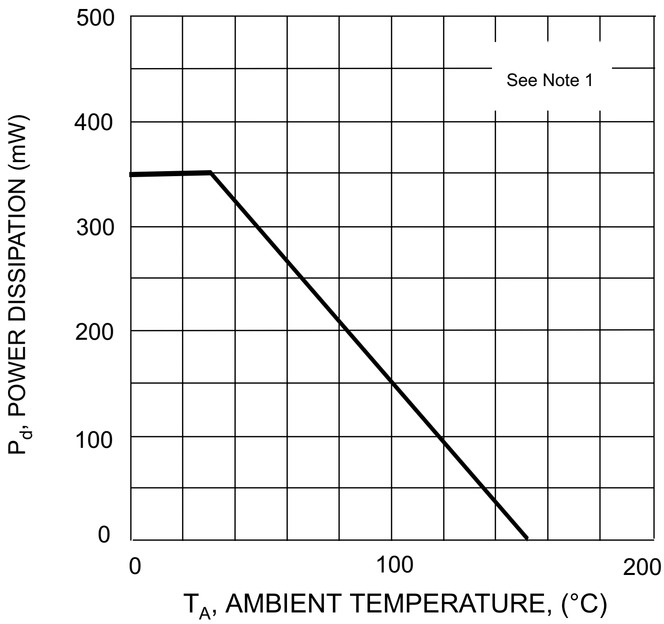


Fig. 1 Power Derating Curve

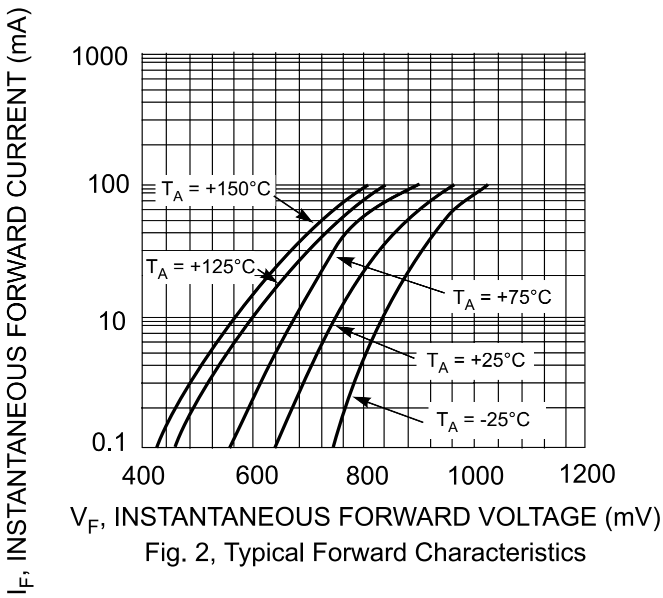


Fig. 2, Typical Forward Characteristics

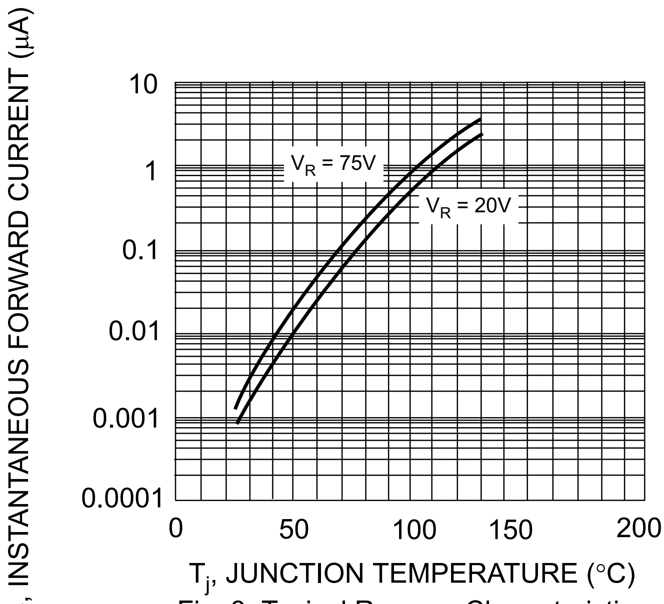


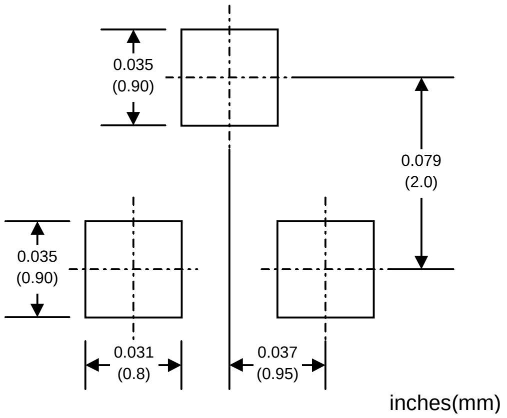
Fig. 3, Typical Reverse Characteristics

ORDERING INFORMATION

Product No.◆	Package Type	Shipping Quantity
BAS16-T1	SOT-23	3000/Tape & Reel
BAS16-T3	SOT-23	10000/Tape & Reel

Products listed in **bold** are WTE **Preferred** devices.
◆T1 suffix refers to a 7” reel. T3 suffix refers to a 13” reel.
Shipping quantity given is for minimum packing quantity only. For minimum order quantity, please consult the Sales Department.

RECOMMENDED FOOTPRINT



Won-Top Electronics Co., Ltd.
No. 44 Yu Kang North 3rd Road, Chine Chen Dist., Kaohsiung, Taiwan
Phone: 886-7-822-5408 or 886-7-822-5410
Fax: 886-7-822-5417
Email: sales@wontop.com
Internet: http://www.wontop.com

National Semiconductor

February 1995

DS55451/2/3/4, DS75451/2/3/4 Series Dual Peripheral Drivers

General Description

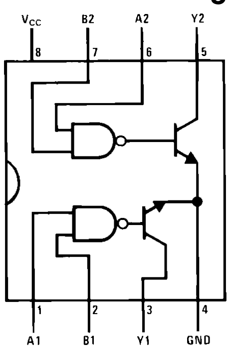
The DS7545X series of dual peripheral drivers is a family of versatile devices designed for use in systems that use TTL logic. Typical applications include high speed logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, bus drivers and memory drivers.

The DS55451/DS75451, DS55452/DS75452, DS55453/DS75453 and DS55454/DS75454 are dual peripheral AND, NAND, OR and NOR drivers, respectively, (positive logic) with the output of the logic gates internally connected to the bases of the NPN output transistors.

Features

- 300 mA output current capability
- High voltage outputs
- No output latch-up at 20V
- High speed switching
- Choice of logic function
- TTL compatible diode-clamped inputs
- Standard supply voltages
- Replaces TI "A" and "B" series

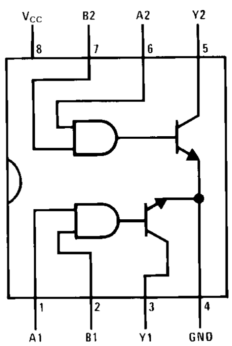
Connection Diagrams (Dual-In-Line and Metal Can Packages)



TL/F/5824–2

Top View

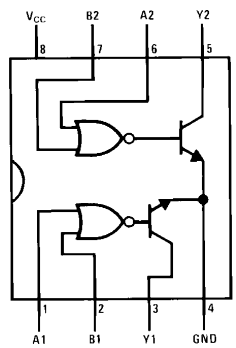
Order Number DS55451J-8, DS75451M or DS75451N



TL/F/5824–3

Top View

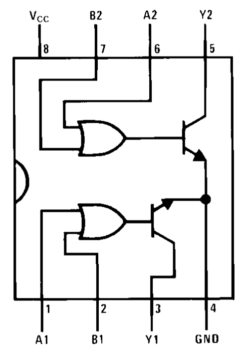
Order Number DS55452J-8, DS75452M or DS75452N



TL/F/5824–4

Top View

Order Number DS55453J-8, DS75453M or DS75453N



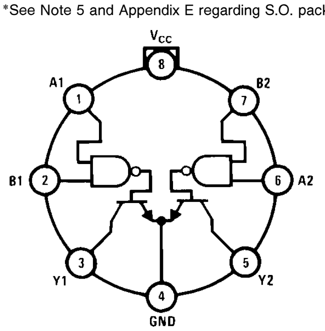
TL/F/5824–5

Top View

Order Number DS55454J-8, DS75454M or DS75454N

See NS Package Numbers J08A, M08A* or N08E

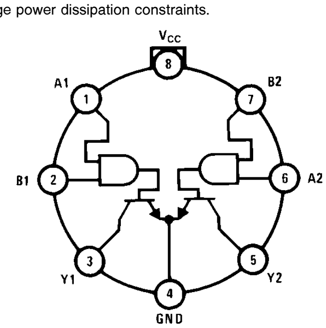
*See Note 5 and Appendix E regarding S.O. package power dissipation constraints.



TL/F/5824–6

Top View

Order Number DS55451H

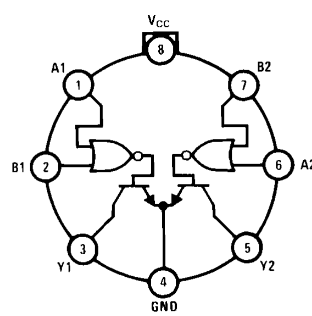


TL/F/5824–7

Top View

(Pin 4 is in Electrical Contact with the Case)

Order Number DS55452H



TL/F/5824–8

Top View

Order Number DS55453H

See NS Package Number H08C

RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, (V_{CC}) (Note 2)	7.0V
Input Voltage	5.5V
Inter-Emitter Voltage (Note 3)	5.5V
Output Voltage (Note 4)	
DS55451/DS75451, DS55452/DS75452, DS55453/DS75453, DS55454/DS75454	30V
Output Current (Note 5)	
DS55451/DS75451, DS55452/DS75452, DS55453/DS75453, DS55454/DS75454	300 mA
DS75451/2/3/4 Maximum Power (Note 5) Dissipation† at 25°C	
Cavity Package	1090 mW
Molded DIP Package	957 mW
TO-5 Package	760 mW
SO Package	632 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage, (V_{CC})			
DS5545X	4.5	5.5	V
DS7545X	4.75	5.25	V
Temperature, (T_A)			
DS5545X	−55	+125	°C
DS7545X	0	+70	°C

† Derate cavity package 7.3 mW/°C above 25°C; derate molded package 7.7 mW/°C above 25°C; derate TO-5 package 5.1 mW/°C above 25°C; derate SO package 7.56 mW/°C above 25°C.

Electrical Characteristics

DS55451/DS75451, DS55452/DS75452, DS55453/DS75453, DS55454/DS75454 (Notes 6 and 7)

Symbol	Parameter	Conditions				Min	Typ	Max	Units
V_{IH}	High-Level Input Voltage	*(Figure 7)*				2			V
V_{IL}	Low-Level Input Voltage							0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA						−1.5	V
V_{OL}	Low-Level Output Voltage	V_{CC} = Min, *(Figure 7)*	V_{IL} = 0.8V	I_{OL} = 100 mA	DS55451, DS55453		0.25	0.5	V
					DS75451, DS75453		0.25	0.4	V
				I_{OL} = 300 mA	DS55451, DS55453		0.5	0.8	V
					DS75451, DS75453		0.5	0.7	V
			V_{IH} = 2V	I_{OL} = 100 mA	DS55452, DS55454		0.25	0.5	V
					DS75452, DS75454		0.25	0.4	V
				I_{OL} = 300 mA	DS55452, DS55454		0.5	0.8	V
					DS75452, DS75454		0.5	0.7	V
I_{OH}	High-Level Output Current	V_{CC} = Min, *(Figure 7)*	V_{OH} = 30V	V_{IH} = 2V	DS55451, DS55453			300	μA
					DS75451, DS75453			100	μA
				V_{IL} = 0.8V	DS55452, DS55454			300	μA
					DS75452, DS75454			100	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V, *(Figure 9)*						1	mA
I_{IH}	High-Level Input Current	V_{CC} = Max, V_I = 2.4V, *(Figure 9)*						40	μA
I_{IL}	Low-Level Input Current	V_{CC} = Max, V_I = 0.4V, *(Figure 8)*					−1	−1.6	mA
I_{CCH}	Supply Current, Outputs High	V_{CC} = Max, *(Figure 10)*	V_I = 5V		DS55451/DS75451		7	11	mA
			V_I = 0V		DS55452/DS75452		11	14	mA
			V_I = 5V		DS55453/DS75453		8	11	mA
			V_I = 0V		DS55454/DS75454		13	17	mA
I_{CCL}	Supply Current, Outputs Low	V_{CC} = Max, *(Figure 10)*	V_I = 0V		DS55451/DS75451		52	65	mA
			V_I = 5V		DS55452/DS75452		56	71	mA
			V_I = 0V		DS55453/DS75453		54	68	mA
			V_I = 5V		DS55454/DS75454		61	79	mA

Switching Characteristics

DS55451/DS75451, DS55452/DS75452, DS55453/DS75453, DS55454/DS75454 (V_{CC} = 5V, T_A = 25°C)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_L = 15 pF, R_L = 50Ω, I_O ≈ 200 mA, *(Figure 14)*	DS55451/DS75451		18	25	ns
			DS55452/DS75452		26	35	ns
			DS55453/DS75453		18	25	ns
			DS55454/DS75454		27	35	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	C_L = 15 pF, R_L = 50Ω, I_O ≈ 200 mA, *(Figure 14)*	DS55451/DS75451		18	25	ns
			DS55452/DS75452		24	35	ns
			DS55453/DS75453		16	25	ns
			DS55454/DS75454		24	35	ns
t_{TLH}	Transition Time, Low-to-High Level Output	C_L = 15 pF, R_L = 50Ω, I_O ≈ 200mA, *(Figure 14)*			5	8	ns
t_{THL}	Transition Time, High-to-Low Level Output	C_L = 15 pF, R_L = 50Ω, I_O ≈ 200 mA, *(Figure 14)*			7	12	ns
V_{OH}	High-Level Output Voltage after Switching	V_S = 20V, I_O ≈ 300 mA, *(Figure 15)*		V_S − 6.5			mV

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Voltage values are with respect to network ground terminal unless otherwise specified.

Note 3: The voltage between two emitters of a multiple-emitter transistor.

Note 4: The maximum voltage which should be applied to any output when it is in the "OFF" state.

Note 5: Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.

Note 6: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS55450 series and across the 0°C to +70°C range for the DS7545X series. All typicals are given for V_{CC} = +5V and T_A = 25°C.

Note 7: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Truth Tables (H = high level, L = low level)

DS55451/DS75451

A	B	Y
L	L	L (ON State)
L	H	L (ON State)
H	L	L (ON State)
H	H	H (OFF State)

DS55453/DS75453

A	B	Y
L	L	L (ON State)
L	H	H (OFF State)
H	L	H (OFF State)
H	H	H (OFF State)

DS55452/DS75452

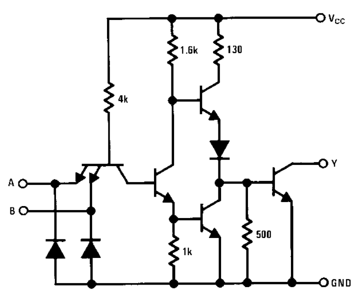
A	B	Y
L	L	H (OFF State)
L	H	H (OFF State)
H	L	H (OFF State)
H	H	L (ON State)

DS55454/DS75454

A	B	Y
L	L	H (OFF State)
L	H	L (ON State)
H	L	L (ON State)
H	H	L (ON State)

Schematic Diagrams

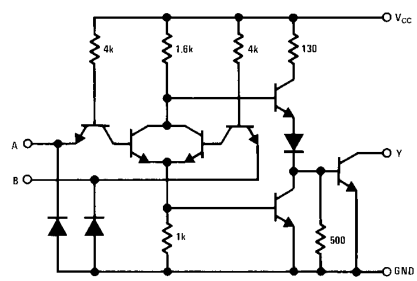
DS55451/DS75451



TL/F/5824–11

Resistor values shown are nominal.

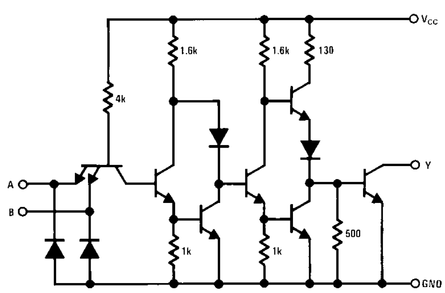
DS55453/DS75453



TL/F/5824–13

Resistor values shown are nominal.

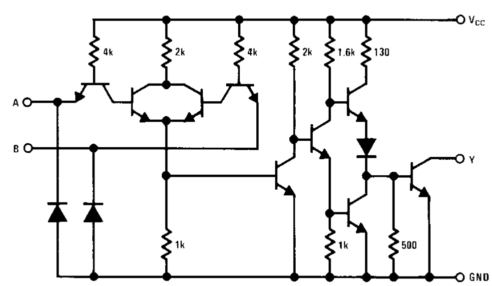
DS55452/DS75452



TL/F/5824–12

Resistor values shown are nominal.

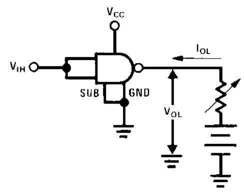
DS55454/DS75454



TL/F/5824–14

Resistor values shown are nominal.

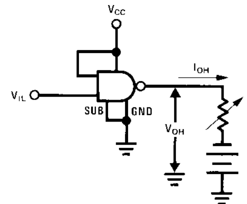
DC Test Circuits



TL/F/5824–15

Both inputs are tested simultaneously.

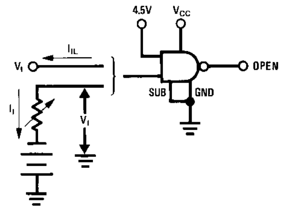
FIGURE 1. V_{IH}, V_{OL}



TL/F/5824–16

Each input is tested separately.

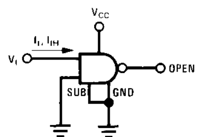
FIGURE 2. V_{IL}, V_{OH}



TL/F/5824–17

Each input is tested separately.

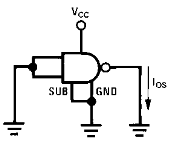
FIGURE 3. V_I, I_{IL}



TL/F/5824–18

Each input is tested separately.

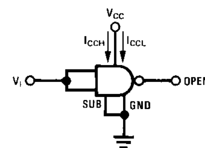
FIGURE 4. I_I, I_{IH}



TL/F/5824–19

Each input is tested separately.

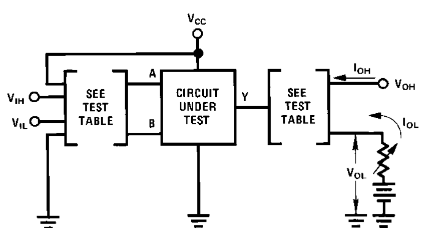
FIGURE 5. I_{OS}



TL/F/5824–20

Both gates are tested simultaneously.

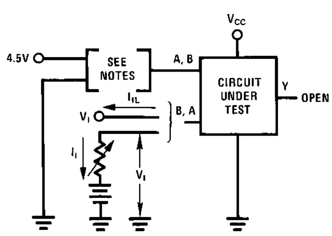
FIGURE 6. I_{CCH}, I_{CCL}



TL/F/5824–21

Circuit	Input Under Test	Other Input	Output	
			Apply	Measure
DS55451	V_{IH}	V_{IH}	V_{OH}	I_{OH}
	V_{IL}	V_{CC}	I_{OL}	V_{OL}
DS55452	V_{IH}	V_{IH}	I_{OL}	V_{OL}
	V_{IL}	V_{CC}	V_{OH}	I_{OH}
DS55453	V_{IH}	Gnd	V_{OH}	I_{OH}
	V_{IL}	V_{IL}	I_{OL}	V_{OH}
DS55454	V_{IH}	Gnd	I_{OL}	V_{OL}
	V_{IL}	V_{IL}	V_{OH}	I_{OH}

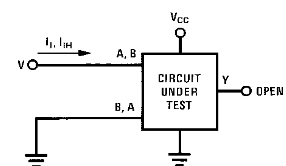
FIGURE 7. V_{IH}, V_{IL}, I_{OH}, V_{OL}



Note A: Each input is tested separately.
Note B: When testing DS55453/DS75453, DS55454/DS75454, input not under test is grounded.
For all other circuits it is at 4.5V.

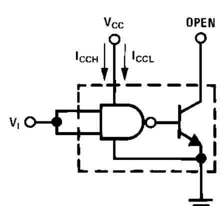
TL/F/5824–22

FIGURE 8. V_I, V_{IL}



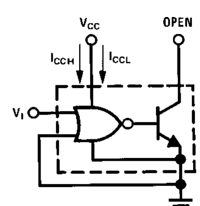
Each input is tested separately. TL/F/5824–23

FIGURE 9. I_I, I_{IH}



Both gates are tested simultaneously. TL/F/5824–24

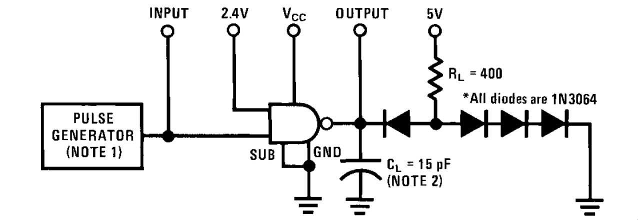
FIGURE 10. I_{CCH}, I_{CCL} for AND, NAND Circuits



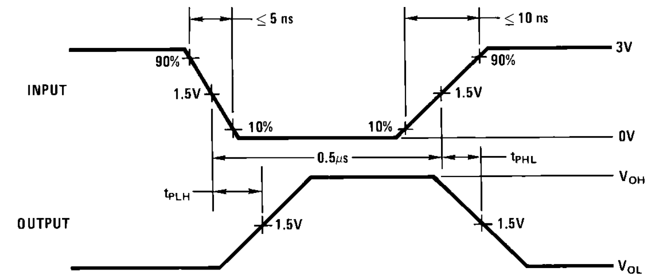
Both gates are tested simultaneously. TL/F/5824–25

FIGURE 11. I_{CCH}, I_{CCL} for OR, NOR Circuits

AC Test Circuits and Switching Time Waveforms



TL/F/5824–26

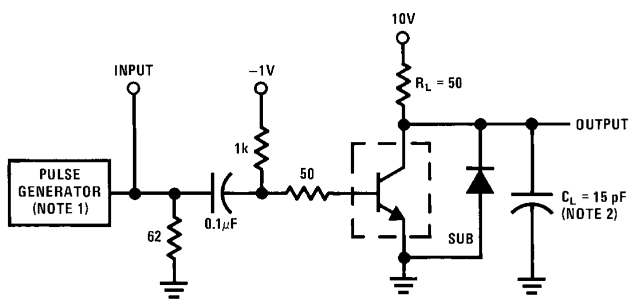


TL/F/5824–27

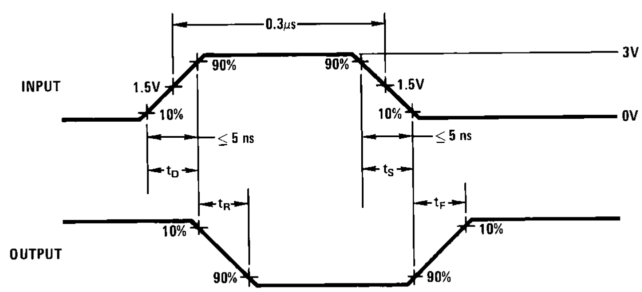
Note 1: The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{OUT} \approx 50\Omega$.

Note 2: C_L includes probe and jig capacitance.

FIGURE 12. Propagation Delay Times, Each Gate



TL/F/5824–28



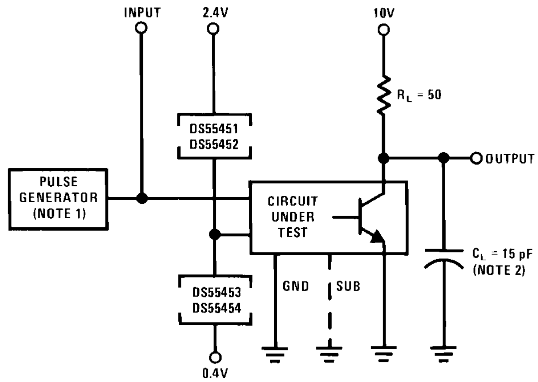
TL/F/5824–29

Note 1: The pulse generator has the following characteristics: duty cycle ≤ 1%, $Z_{OUT} \approx 50\Omega$.

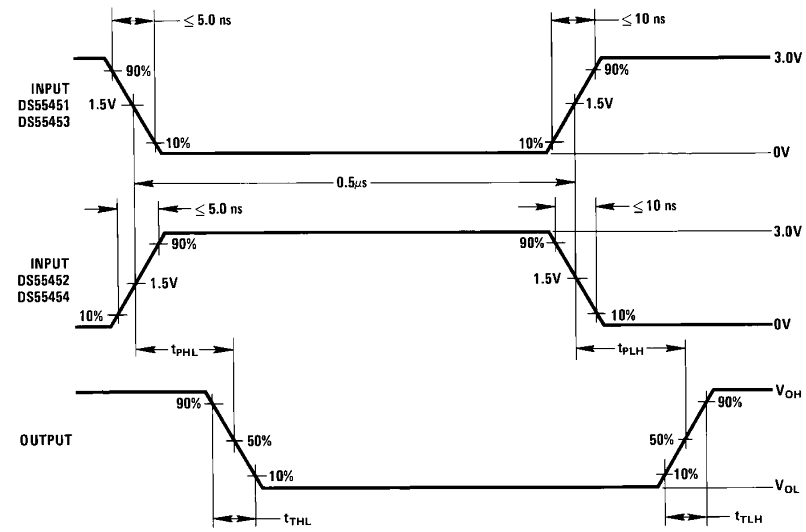
Note 2: C_L includes probe and jig capacitance.

FIGURE 13. Switching Times, Each Transistor

AC Test Circuits and Switching Time Waveforms (Continued)



TL/F/5824–30



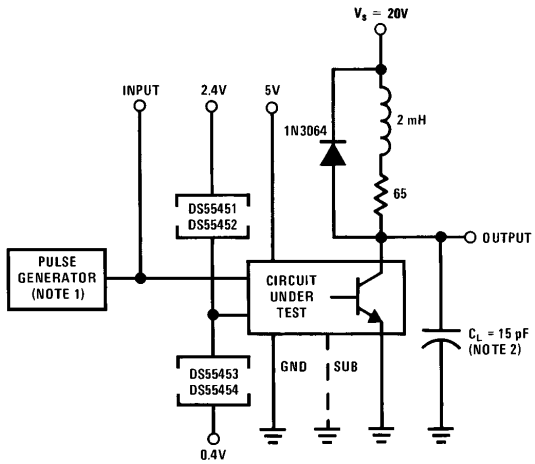
Note 1: The pulse generator has the following characteristics: PRR = 1.0 MHz, Z_{OUT} ≈ 50Ω.

TL/F/5824–31

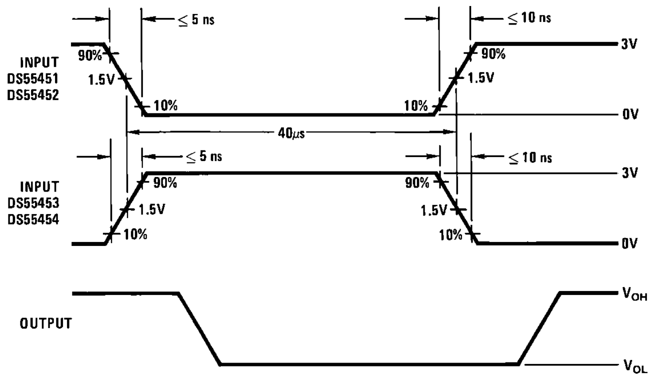
Note 2: C_L includes probe and jig capacitance.

FIGURE 14. Switching Times of Complete Drivers

AC Test Circuits and Switching Time Waveforms (Continued)



TL/F/5824–32



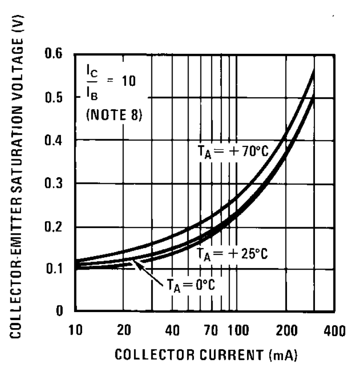
TL/F/5824–33

Note 1: The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_{OUT} ≈ 50Ω.

Note 2: C_L includes probe and jig capacitance.

FIGURE 15. Latch-UP Test of Complete Drivers

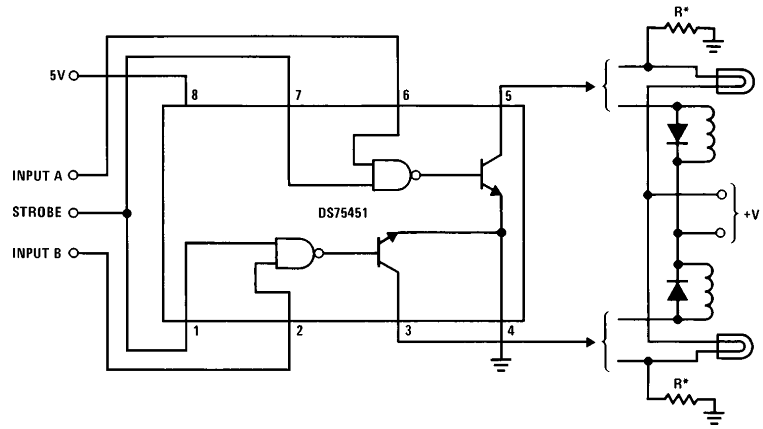
Typical Performance Characteristics



TL/F/5824–37

FIGURE 16. Transistor Collector-Emitter Saturation Voltage vs Collector Current

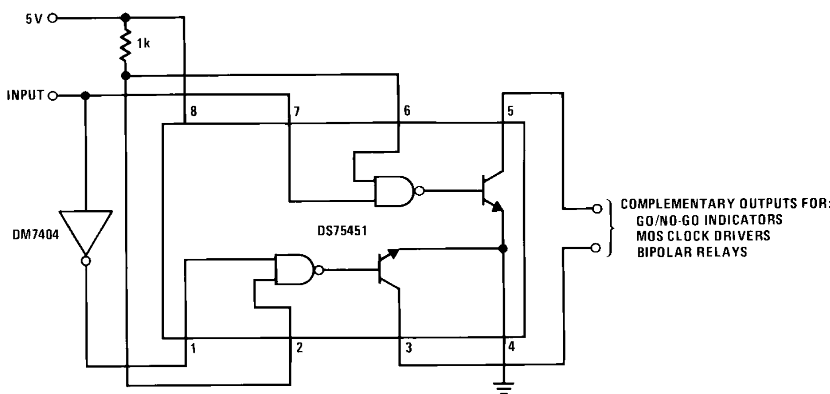
Typical Applications



TL/F/5824–46

*Optional keep-alive resistors maintain off-state lamp current at ≈ 10% to reduce surge current.

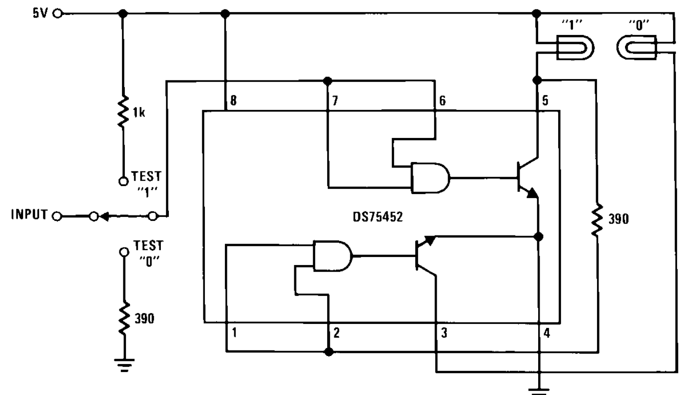
FIGURE 17. Dual Lamp or Relay Driver



TL/F/5824–47

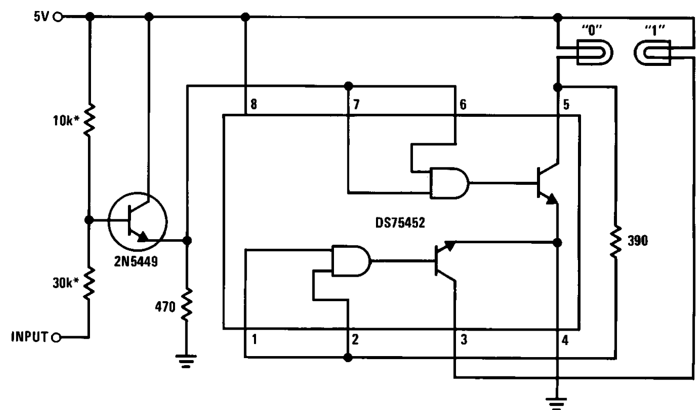
FIGURE 18. Complementary Driver

Typical Applications (Continued)



TL/F/5824–48

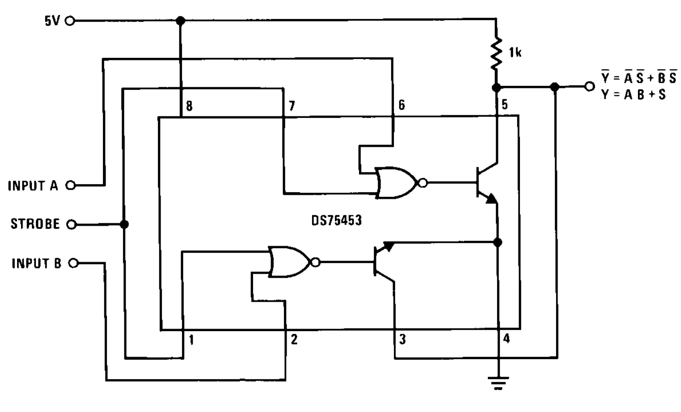
FIGURE 19. TTL or DTL Positive Logic-Level Detector



TL/F/5824–49

*The two input resistors must be adjusted for the level of MOS input.

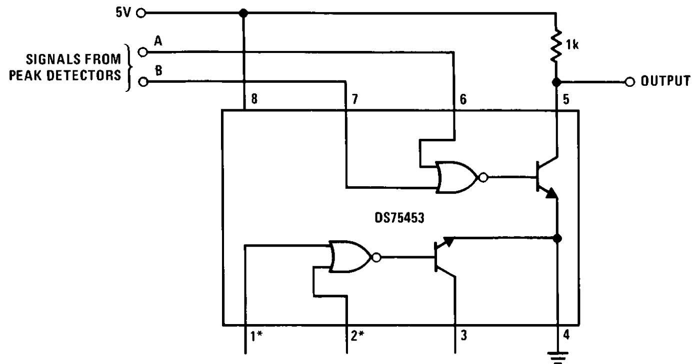
FIGURE 20. MOS Negative Logic-Level Detector



TL/F/5824–50

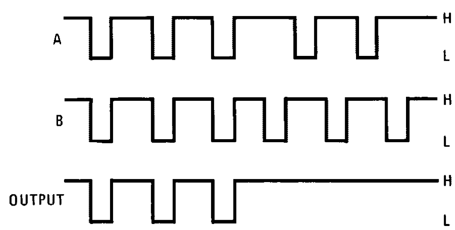
FIGURE 21. Logic Signal Comparator

Typical Applications (Continued)



TL/F/5824–51

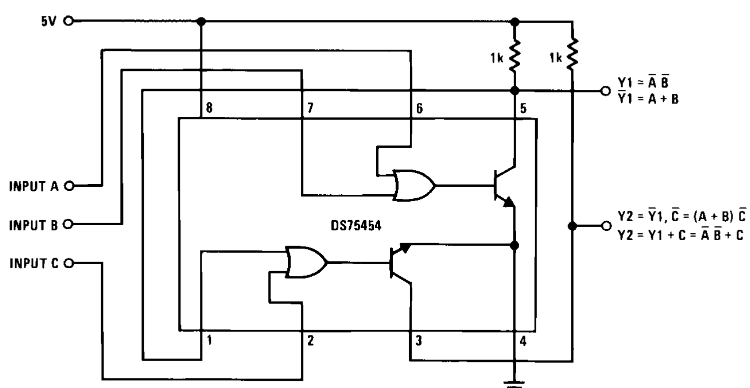
*If inputs are unused, they should be connected to +5V through a 1k resistor.



TL/F/5824–52

Low output occurs only when inputs are low simultaneously.

FIGURE 22. In-Phase Detector



TL/F/5824–53

FIGURE 23. Multifunction Logic-Signal Comparator

Typical Applications (Continued)

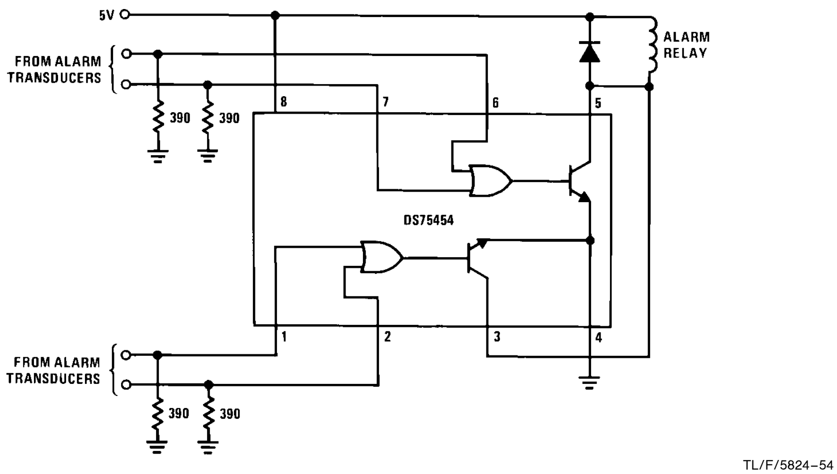
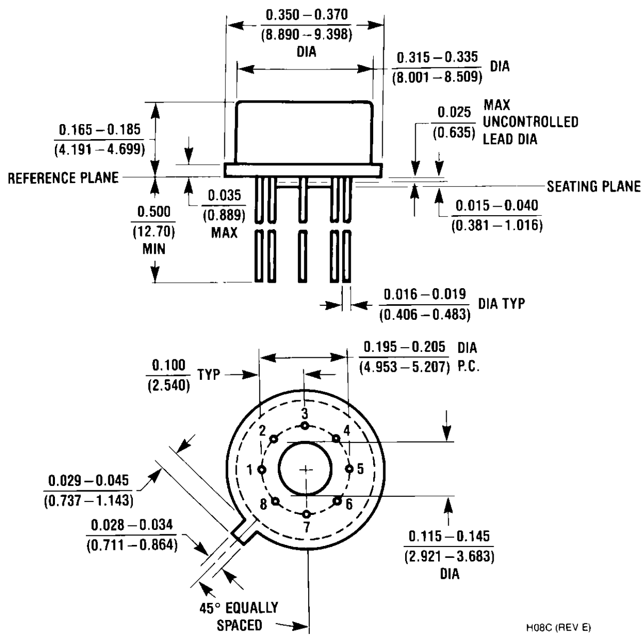
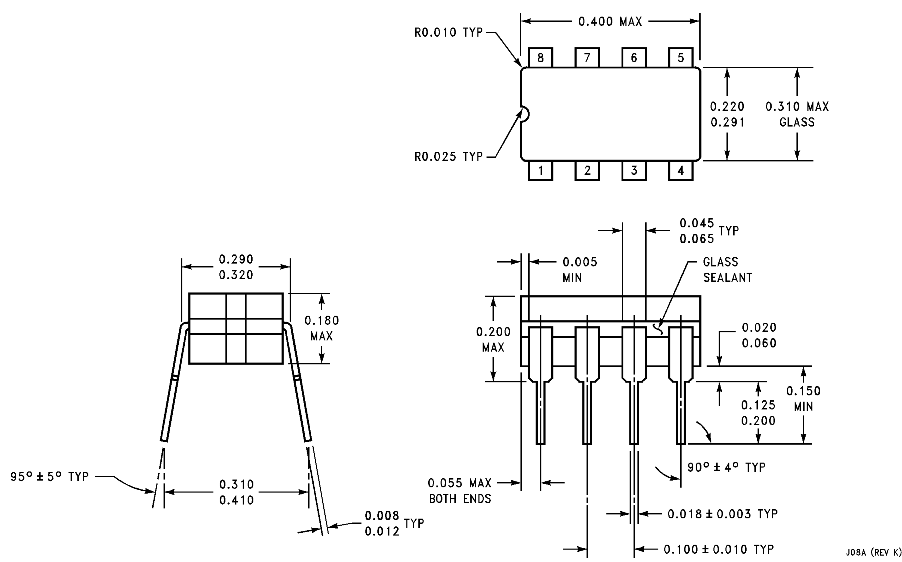


FIGURE 24. Alarm Detector

Physical Dimensions inches (millimeters)

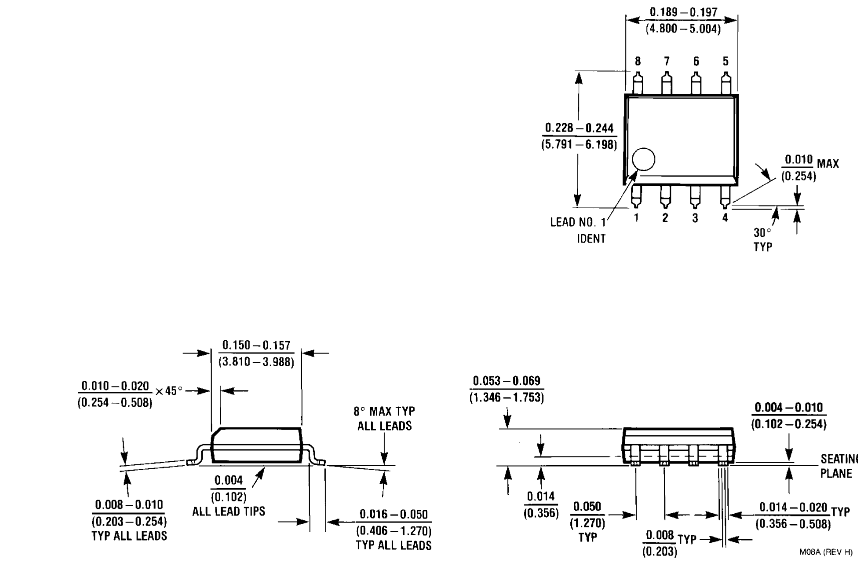


Metal Can Package (H)
Order Number DS55451H, DS55452H or DS55453H,
NS Package Number H08C

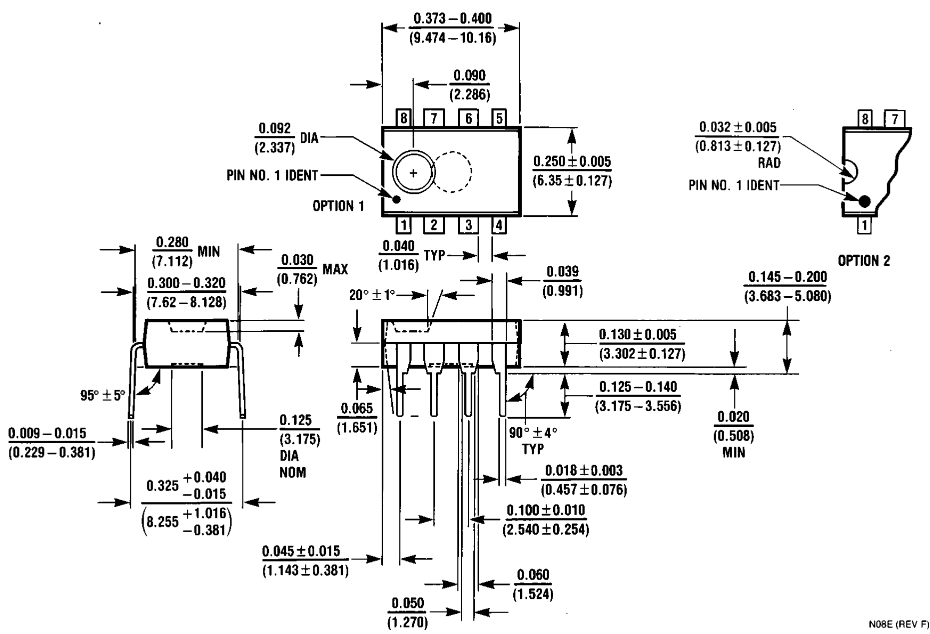


Ceramic Dual-In-Line Package (J)
Order Number DS55451J-8, DS55452J-8,
DS55453J-8 or DS55454J-8
NS Package Number J08A

Physical Dimensions inches (millimeters) (Continued)



SO Package (M)
Order Number DS75451M, DS75452M, DS75453M or DS75454M
NS Package Number M08A



Molded Dual-In-Line Package (N)
Order Number DS75451N, DS75452N, DS75453N, DS75454N
NS Package Number N08E

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Fax: 81-043-299-2408

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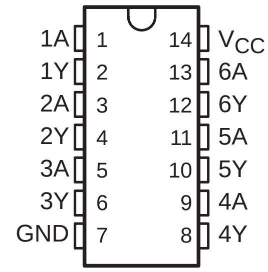
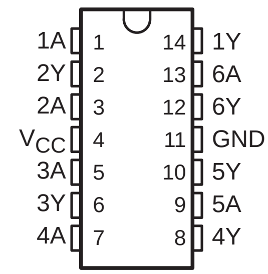
description/ordering information

These devices contain six independent inverters.

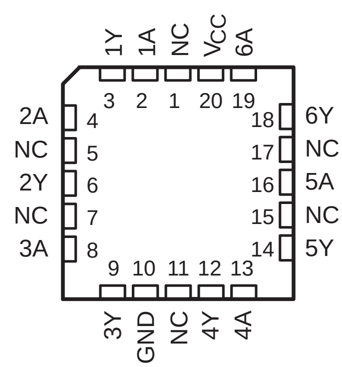
SN5404 . . . J PACKAGE
SN54LS04, SN54S04 . . . J OR W PACKAGE
SN7404, SN74S04 . . . D, N, OR NS PACKAGE
SN74LS04 . . . D, DB, N, OR NS PACKAGE
(TOP VIEW)



SN5404 . . . W PACKAGE
(TOP VIEW)



SN54LS04, SN54S04 . . . FK PACKAGE
(TOP VIEW)



NC − No internal connection

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ORDERING INFORMATION

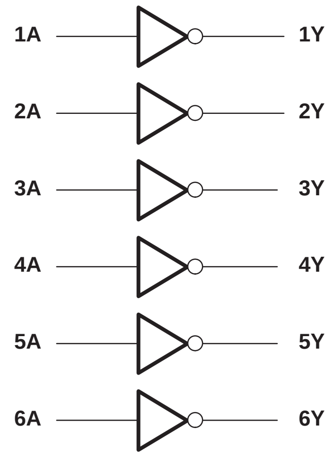
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP − N	Tube	SN7404N	SN7404N
		Tube	SN74LS04N	SN74LS04N
		Tube	SN74S04N	SN74S04N
	SOIC − D	Tube	SN7404D	7404
		Tape and reel	SN7404DR	
		Tube	SN74LS04D	LS04
		Tape and reel	SN74LS04DR	
		Tube	SN74S04D	S04
		Tape and reel	SN74S04DR	
	SOP − NS	Tape and reel	SN7404NSR	SN7404
		Tape and reel	SN74LS04NSR	74LS04
		Tape and reel	SN74S04NSR	74S04
	SSOP − DB	Tape and reel	SN74LS04DBR	LS04
−55°C to 125°C	CDIP − J	Tube	SN5404J	SN5404J
		Tube	SNJ5404J	SNJ5404J
		Tube	SN54LS04J	SN54LS04J
		Tube	SN54S04J	SN54S04J
		Tube	SNJ54LS04J	SNJ54LS04J
		Tube	SNJ54S04J	SNJ54S04J
	CFP − W	Tube	SNJ5404W	SNJ5404W
		Tube	SNJ54LS04W	SNJ54LS04W
		Tube	SNJ54S04W	SNJ54S04W
	LCCC − FK	Tube	SNJ54LS04FK	SNJ54LS04FK
		Tube	SNJ54S04FK	SNJ54S04FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

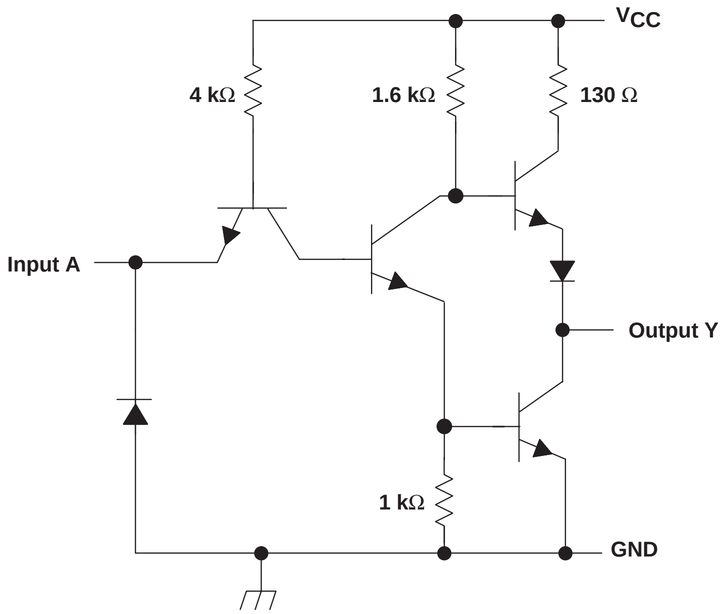
logic diagram (positive logic)



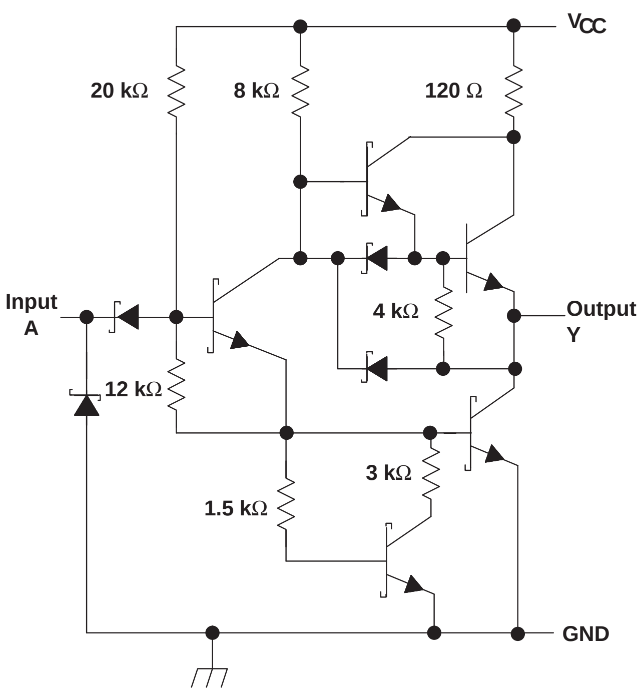
$Y = \overline{A}$

schematics (each gate)

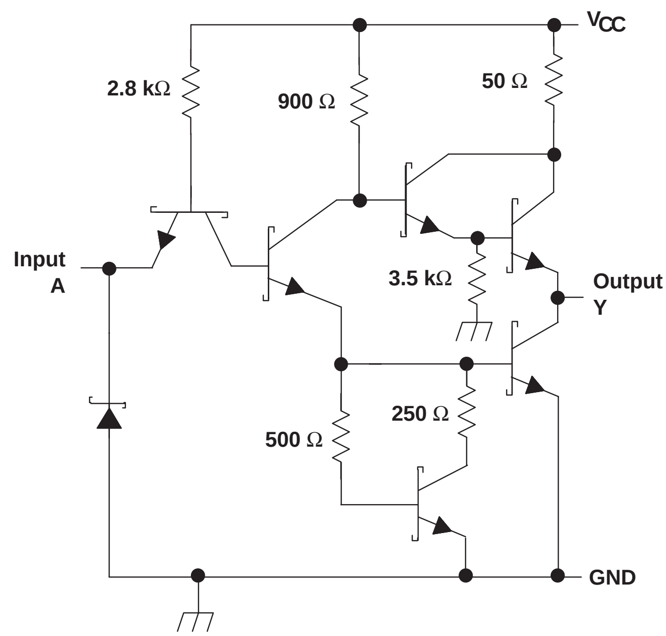
’04



’LS04



’S04



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . 7 V
Input voltage, V_I: ’04, ’S04 . . . . 5.5 V
’LS04 . . . . 7 V
Package thermal impedance, θ_{JA} (see Note 2): D package . . . . 86°C/W
DB package . . . . 96°C/W
N package . . . . 80°C/W
NS package . . . . 76°C/W
Storage temperature range, T_{stg} . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. This are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values are with respect to network ground terminal.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		SN5404			SN7404			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			16			16	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡			SN5404			SN7404			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −12 mA				−1.5			−1.5	V
V_{OH}	V_{CC} = MIN,	V_{IL} = 0.8 V,	I_{OH} = −0.4 mA	2.4	3.4		2.4	3.4		V
V_{OL}	V_{CC} = MIN,	V_{IH} = 2 V,	I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	V_{CC} = MAX,	V_I = 5.5 V				1			1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.4 V				40			40	µA
I_{IL}	V_{CC} = MAX,	V_I = 0.4 V				−1.6			−1.6	mA
I_{OS}¶	V_{CC} = MAX			−20		−55	−18		−55	mA
I_{CCH}	V_{CC} = MAX,	V_I = 0 V			6	12		6	12	mA
I_{CCL}	V_{CC} = MAX,	V_I = 4.5 V			18	33		18	33	mA

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.
¶ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN5404 SN7404			UNIT
				MIN	TYP	MAX	
t_{PLH}	A	Y	R_L = 400 Ω, C_L = 15 pF		12	22	ns
t_{PHL}					8	15	

recommended operating conditions (see Note 3)

		SN54LS04			SN74LS04			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			SN54LS04			SN74LS04			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}	V_{CC} = MIN,	V_{IL} = MAX,	I_{OH} = −0.4 mA	2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC} = MIN,	V_{IH} = 2 V	I_{OL} = 4 mA		0.25	0.4			0.4	V
			I_{OL} = 8 mA					0.25	0.5	
I_I	V_{CC} = MAX,	V_I = 7 V				0.1			0.1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V				20			20	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}§	V_{CC} = MAX			−20		−100	−20		−100	mA
I_{CCH}	V_{CC} = MAX,	V_I = 0 V			1.2	2.4		1.2	2.4	mA
I_{CCL}	V_{CC} = MAX,	V_I = 4.5 V			3.6	6.6		3.6	6.6	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54LS04 SN74LS04			UNIT
				MIN	TYP	MAX	
t_{PLH}	A	Y	R_L = 2 kΩ, C_L = 15 pF		9	15	ns
t_{PHL}					10	15	

recommended operating conditions (see Note 3)

		SN54S04			SN74S04			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

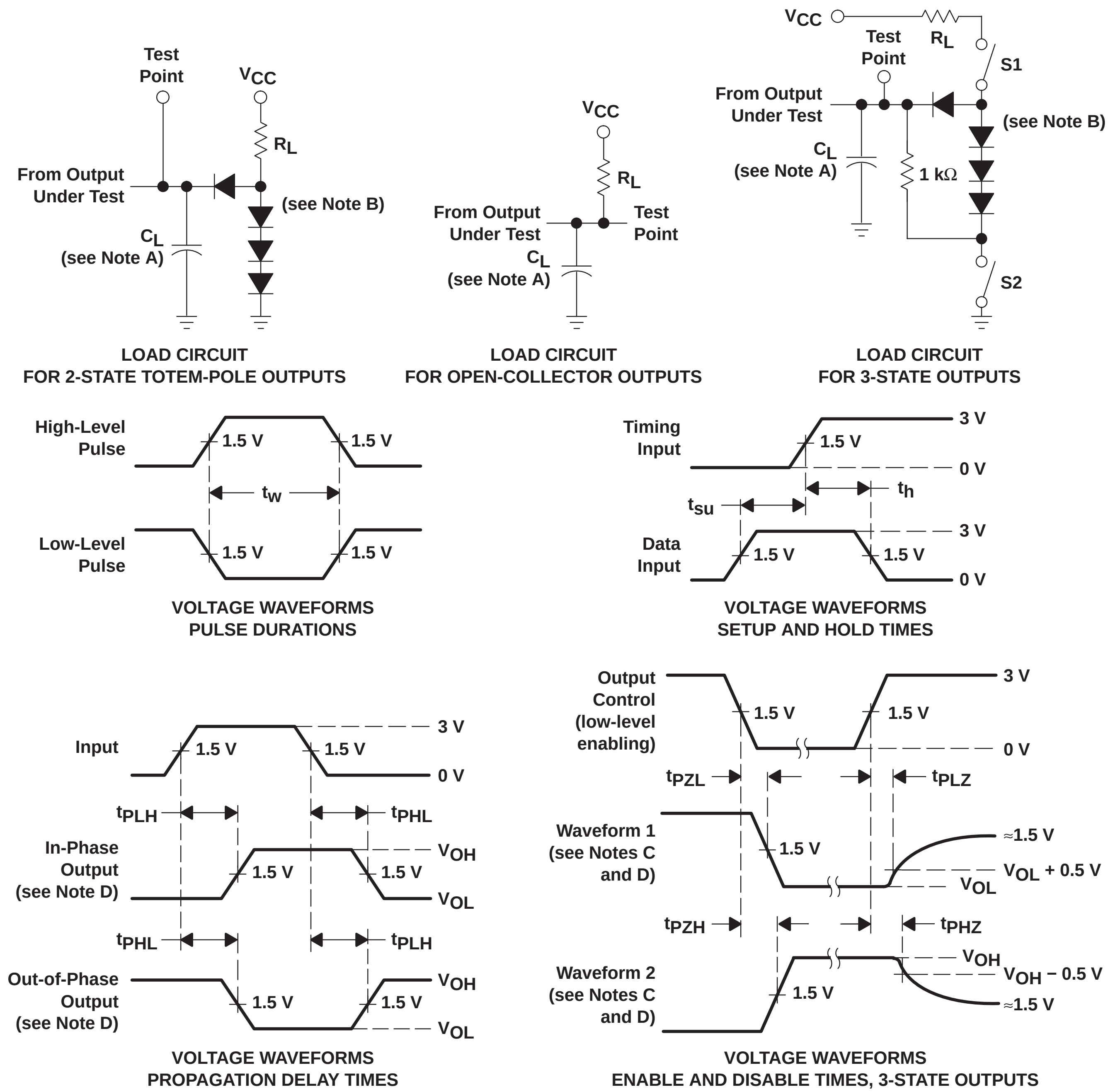
PARAMETER	TEST CONDITIONS†			SN54S04			SN74S04			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA				−1.2			−1.2	V
V_{OH}	V_{CC} = MIN,	V_{IL} = 0.8 V,	I_{OH} = −1 mA	2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC} = MIN,	V_{IH} = 2 V,	I_{OL} = 20 mA			0.5			0.5	V
I_I	V_{CC} = MAX,	V_I = 5.5 V				1			1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V				50			50	µA
I_{IL}	V_{CC} = MAX,	V_I = 0.5 V				−2			−2	mA
I_{OS}§	V_{CC} = MAX			−40		−100	−40		−100	mA
I_{CCH}	V_{CC} = MAX,	V_I = 0 V			15	24		15	24	mA
I_{CCL}	V_{CC} = MAX,	V_I = 4.5 V			30	54		30	54	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		SN54S04 SN74S04			UNIT
					MIN	TYP	MAX	
t_{PLH}	A	Y	R_L = 280 Ω,	C_L = 15 pF		3	4.5	ns
t_{PHL}						3	5	
t_{PLH}	A	Y	R_L = 280 Ω,	C_L = 50 pF		4.5		ns
t_{PHL}						5		

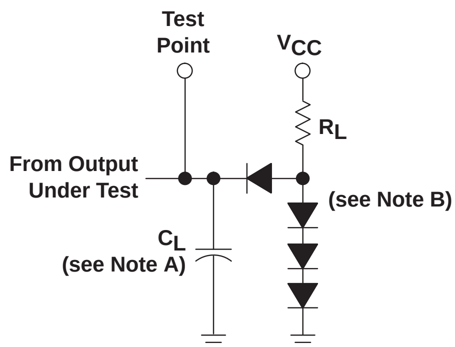
PARAMETER MEASUREMENT INFORMATION
SERIES 54/74 AND 54S/74S DEVICES



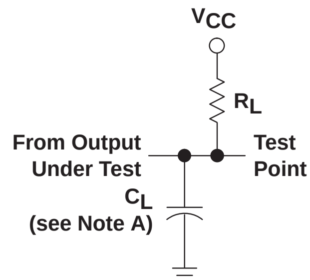
NOTES:
- A. C_L includes probe and jig capacitance.
- B. All diodes are 1N3064 or equivalent.
- C. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- D. S1 and S2 are closed for t_{PLH}, t_{PHL}, t_{PHZ}, and t_{PLZ}; S1 is open and S2 is closed for t_{PZH}; S1 is closed and S2 is open for t_{PZL}.
- E. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O \approx 50\ \Omega$; t_r and $t_f \leq 7$ ns for Series 54/74 devices and t_r and $t_f \leq 2.5$ ns for Series 54S/74S devices.
- F. The outputs are measured one at a time, with one input transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

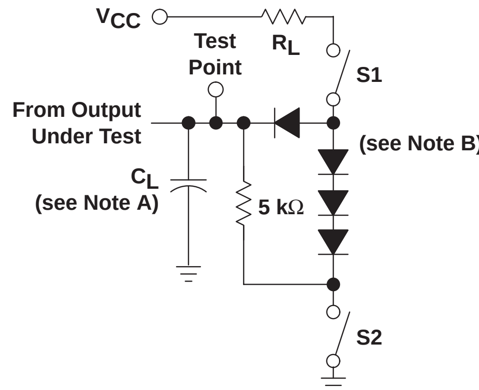
PARAMETER MEASUREMENT INFORMATION
SERIES 54LS/74LS DEVICES



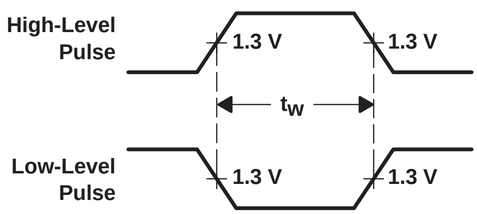
LOAD CIRCUIT
FOR 2-STATE TOTEM-POLE OUTPUTS



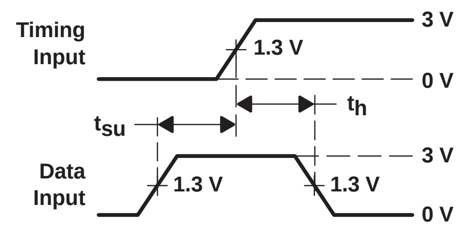
LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS



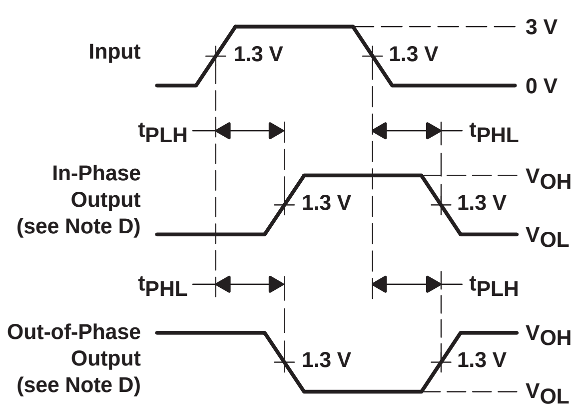
LOAD CIRCUIT
FOR 3-STATE OUTPUTS



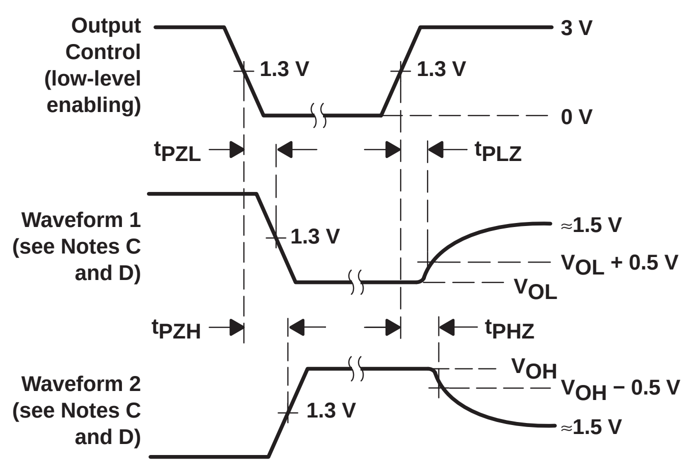
VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES:
A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
D. S1 and S2 are closed for t_{PLH}, t_{PHL}, t_{PHZ}, and t_{PLZ}; S1 is open and S2 is closed for t_{PZH}; S1 is closed and S2 is open for t_{PZL}.
E. Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.
F. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O ≈ 50 Ω, t_r ≤ 1.5 ns, t_f ≤ 2.6 ns.
G. The outputs are measured one at a time, with one input transition per measurement.

Figure 2. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
JM38510/00105BCA	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
JM38510/00105BDA	ACTIVE	CFP	W	14	1	None	Call TI	Level-NC-NC-NC
JM38510/07003BCA	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
JM38510/30003B2A	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
JM38510/30003BCA	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
JM38510/30003BDA	ACTIVE	CFP	W	14	1	None	Call TI	Level-NC-NC-NC
JM38510/30003SCA	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
JM38510/30003SDA	ACTIVE	CFP	W	14	1	None	Call TI	Level-NC-NC-NC
SN5404J	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
SN54LS04J	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
SN54S04J	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
SN7404D	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN7404DR	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN7404N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN7404N3	OBSOLETE	PDIP	N	14		None	Call TI	Call TI
SN7404NSR	ACTIVE	SO	NS	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74LS04D	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74LS04DR	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74LS04J	OBSOLETE	CDIP	J	14		None	Call TI	Call TI
SN74LS04N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS04N3	OBSOLETE	PDIP	N	14		None	Call TI	Call TI
SN74LS04NSR	ACTIVE	SO	NS	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74S04D	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74S04DR	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74S04N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74S04N3	OBSOLETE	PDIP	N	14		None	Call TI	Call TI
SN74S04NSR	ACTIVE	SO	NS	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SNJ5404J	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
SNJ5404W	ACTIVE	CFP	W	14	1	None	Call TI	Level-NC-NC-NC
SNJ54LS04FK	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
SNJ54LS04J	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
SNJ54LS04W	ACTIVE	CFP	W	14	1	None	Call TI	Level-NC-NC-NC
SNJ54S04FK	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
SNJ54S04J	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SNJ54S04W	ACTIVE	CFP	W	14	1	None	Call TI	Level-NC-NC-NC

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
None: Not yet available Lead (Pb-Free).
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

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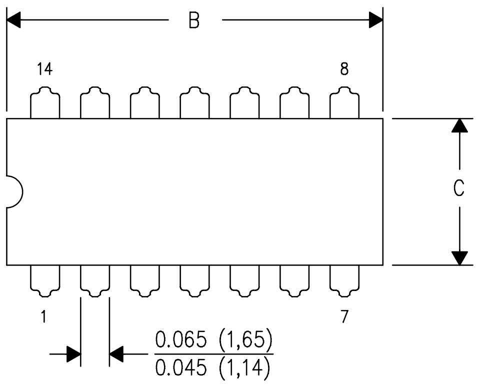
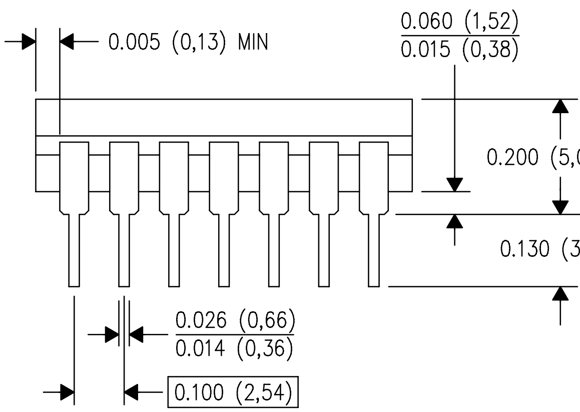
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

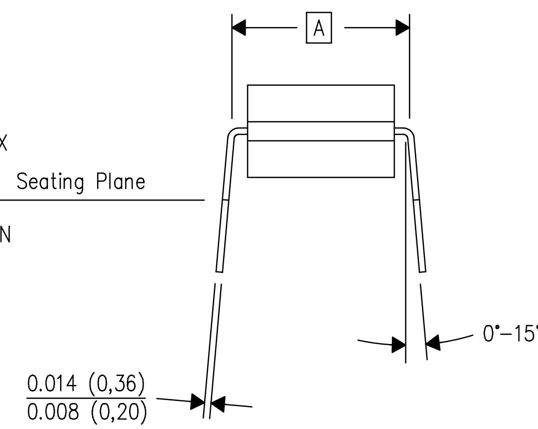
J (R-GDIP-T**) CERAMIC DUAL IN-LINE PACKAGE

14 LEADS SHOWN



PINS ** / DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

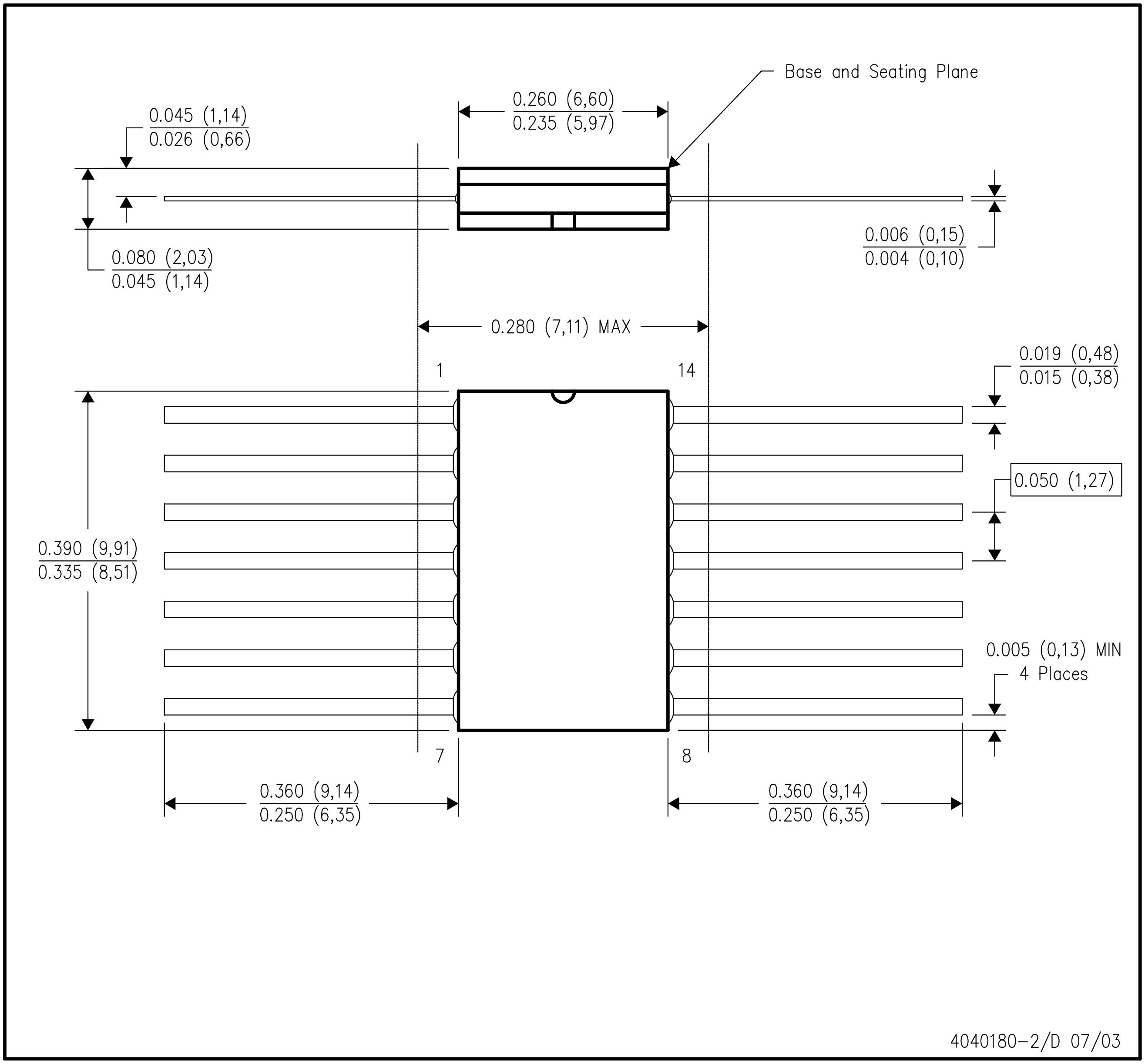




4040083/F 03/03

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

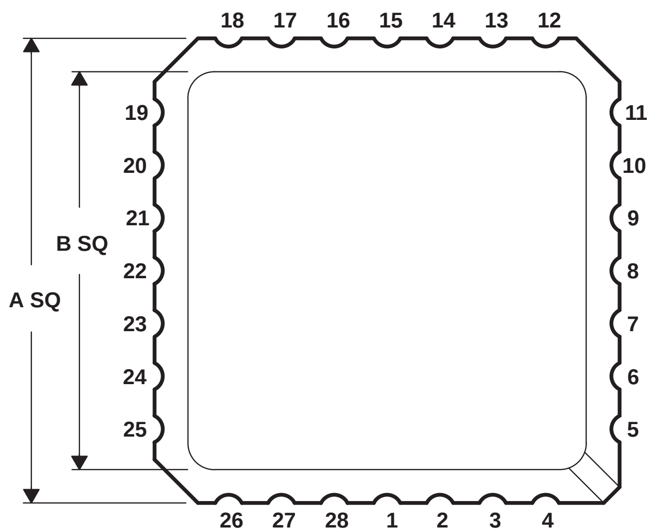
W (R-GDFP-F14) CERAMIC DUAL FLATPACK



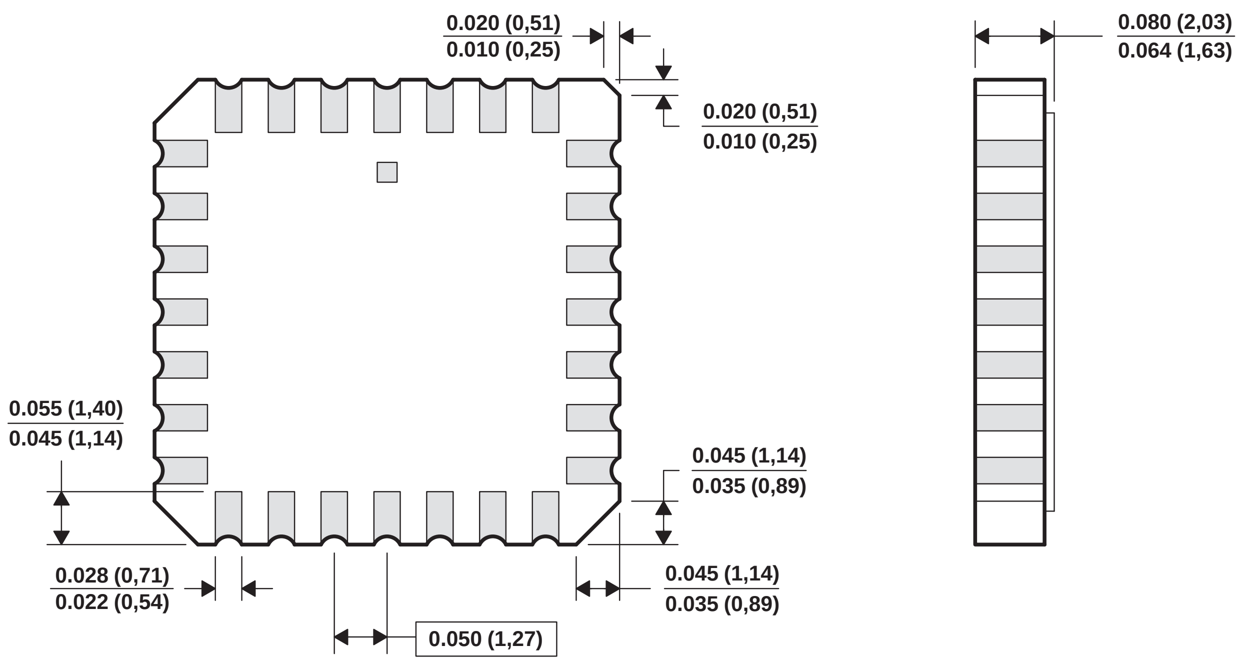
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

FK (S-CQCC-N)** **LEADLESS CERAMIC CHIP CARRIER**

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

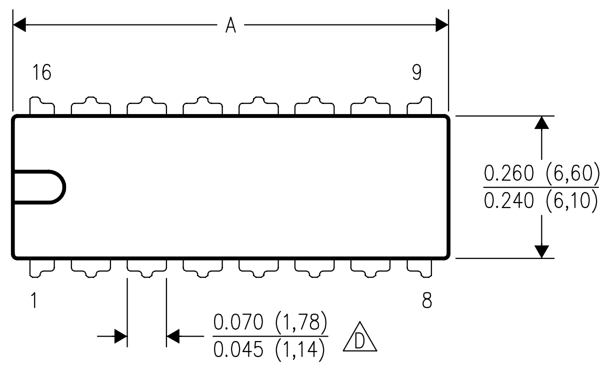


4040140 / D 10/96

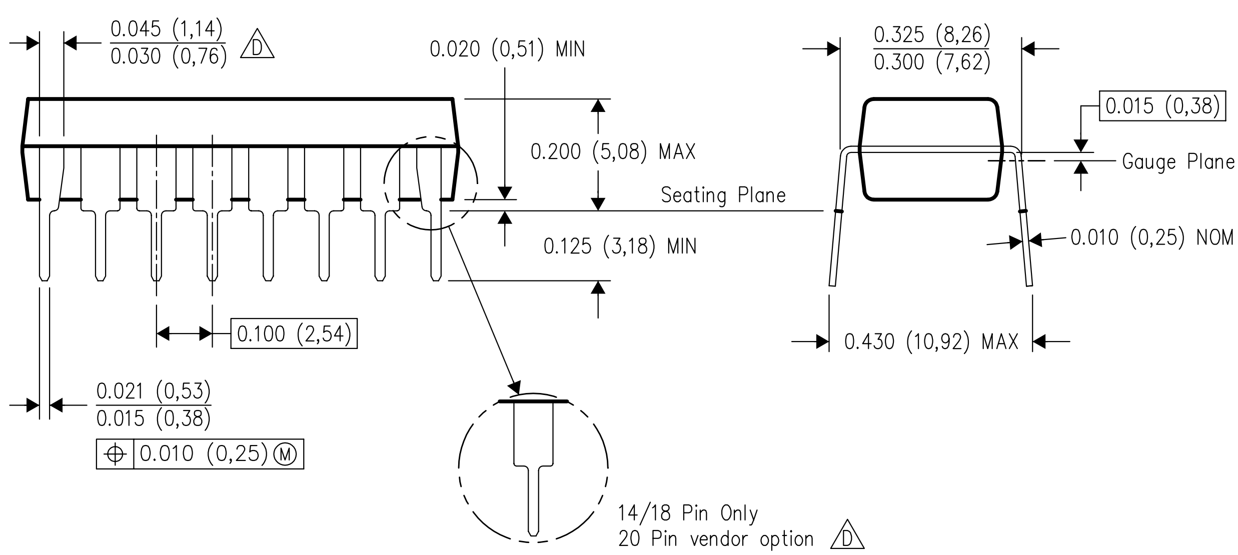
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



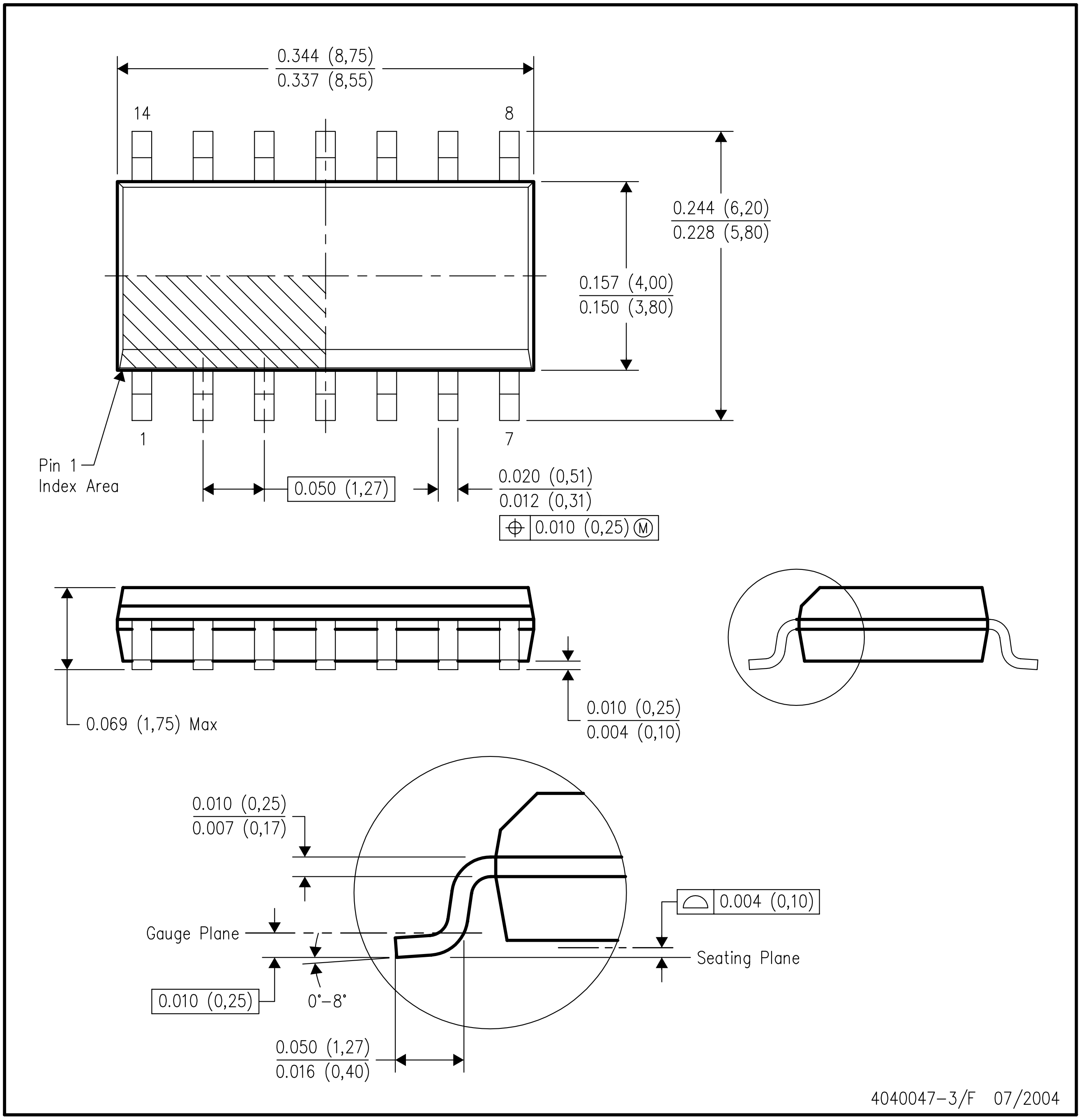
PINS ** / DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
(C) MS–001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
(C) Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
(D) The 20 pin end lead shoulder width is a vendor option, either half or full width.

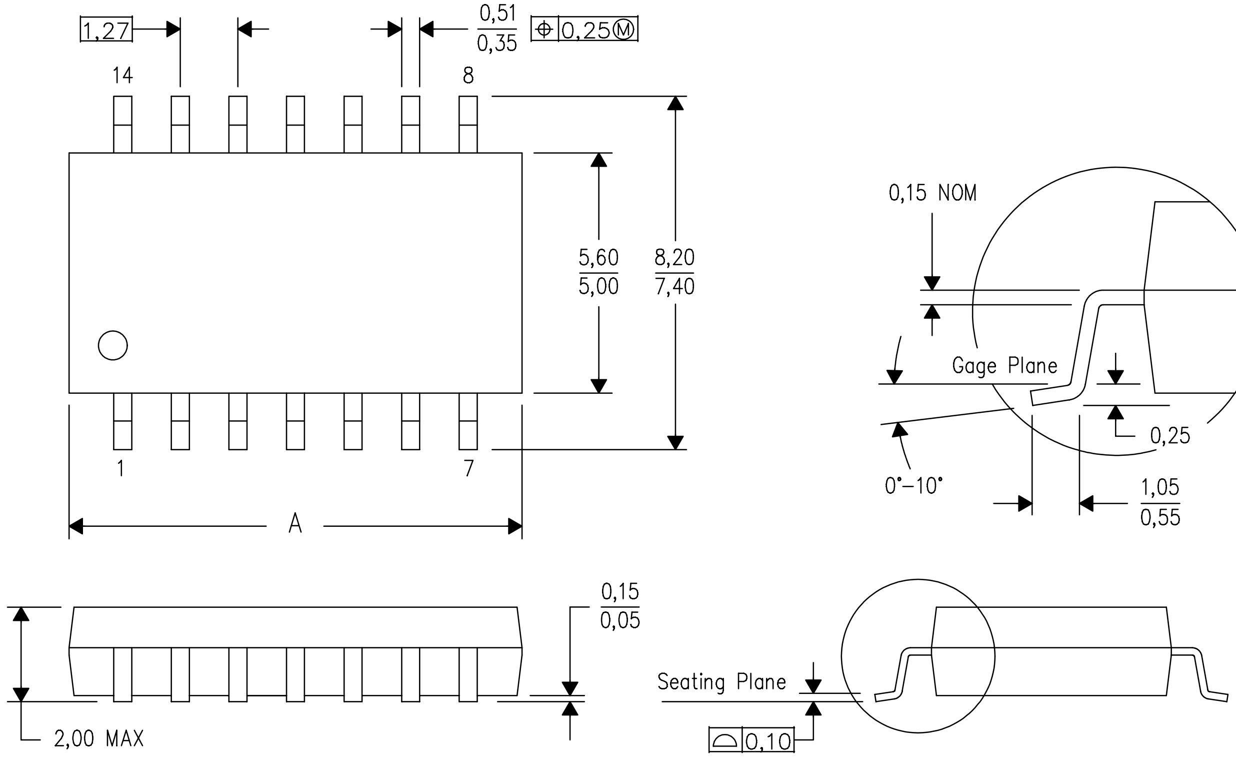
D (R–PDSO–G14) PLASTIC SMALL–OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–012 variation AB.

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



PINS ** / DIM	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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