Development and Prototyping of a Cryogenic IF Low Noise Amplifier: Final Project Report

ESO Contract 79226/17/81324/ASP
WP 7000 – DRD 09

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LIST OF ACRONYMS

2SB	Sideband Separating
ALMA	Atacama Large Millimetre and submillimetre Array
CA	Cold Attenuator
CW	Continuous Wave
CNIG	Centro Nacional de Información Geográfica
DC	Direct Current
DRD	Document Requirement Description
DSB	Double Sideband
DUT	Device Under Test
ESA	European Space Agency
ESO	European Southern Observatory
ETH	Eidgenössische Technische Hochschule (Swiss Federal Polytechnic Institute)
fA	fully Accomplished
FPA	Focal Plane Array
GaAs	Gallium Arsenide
HEMT	High Electron Mobility Transistor
IF	Intermediate frequency
InP	Indium Phosphide
IRAM	Institut de Radioastronomie Millimétrique
IRL	Input Return Loss
IRR	Image Rejection Ratio
LNA	Low Noise Amplifier
MIS	Metal Insulator Semiconductor
MMIC	Monolithic Microwave Integrated Circuit
nA	not Accomplished
NFM	Noise Figure Meter
ORL	Output Return Loss
P1dB	1 dB compression point
pA	partially Accomplished
PDK	Product Design Kit
PN	Part Number
RAMS	Reliability, Availability, Maintainability, and Safety
RF	Radio Frequency
RT	Room Temperature
SIS	Superconductor-Insulator-Superconductor
SoW	Statement of Work
SRF	Self Resonance Frequency
TRL	Technological Readiness Level
TMP	Technical and Management Proposal
VNA	Vector Network Analyzer
VTCL	Variable Temperature Cryogenic Load
WP	Work Package

CONTENTS

1 INTRODUCTION

1.1 SCOPE

This document reports on the final outcome of the study for the "Development and Prototyping of a Cryogenic IF Low-Noise Amplifier", under ESO contract 79226/17/81324/ASP in the framework of ESO Technology Development Project "Cryogenic Amplifier for Advanced ALMA Receivers", as described in the Technical and Management Proposal [1] presented by Yebes Observatory[1]. It is Deliverable Document DRD 09 and represent milestone M9 of the project according to the Statement of Work [2].

The report summarizes the findings and the results achieved during the development of the project, as well as it tries to describe the works done in the design and manufacturing phases. The preceding reports of this project will be cited here for the sake of conciseness; however, following the recommendations of the reviewers of these reports, this document aims to be as self-contained as possible. Therefore, some of the content included here has been taken from previous reports to be presented in a summarized and orderly manner.

1.2 GOALS, MOTIVATION AND STATE-OF-THE-ART

The goal of this project was to explore the limits of the existing technology for the development of a cryogenic amplifier with extremely large fractional bandwidth (16 GHz between 0.1 and 24 GHz) which at the same time should attain state-of-the-art performance in noise temperature (4 K) and input reflection (-15 dB) with a power dissipation below 9 mW. The simultaneous fulfillment of all these specifications is extremely ambitious; a noise temperature below 4 K in a 16 GHz wide band had never been achieved even without the conflicting requirement of -15 dB of input reflection. As stated in the SoW [2], "given the research nature of this activity the technical specifications should be considered as a guideline for the performance to be achieved and will not serve as simple compliance criteria for judging acceptance."

For a complete list of the specifications refer to the first design report [3] and to the Technical Specification document [4]. Table 3 in section 5.2 of this report will contrast the electrical specifications with the results of the final unit.

Such an amplifier perfectly addresses the top development priority of ALMA 2030 roadmap [5]: the expansion of the actual receiver instantaneous bandwidths up to a fourfold increase when combined with 2SB mixers. Most ALMA bands have now a total of 8 GHz per polarization, typically featuring either 4-8 GHz IF LNAs in 2SB receivers or 4-12 GHz IF LNAs in DSB receivers. A 2SB scheme with a 16 GHz bandwidth LNA would deliver 32 GHz per polarization. Furthermore, the input reflection level required would permit the direct connection of the amplifier with the mixer, avoiding a lossy and bulky isolator used in many ALMA bands. This fact, combined with the goal of reducing the noise temperature with respect to the present generation of IF LNAs, would improve the sensitivity of the receivers. Overall, this upgrade would greatly benefit the productivity of the instrument, especially for spectral line surveys, and would also allow blind redshift observations and higher sensitivity continuum observations.

Coming back to the difficulty of designing an amplifier with such ambitious goals, we have compiled in Table 1 a summary of the performance of the best ultra-wideband amplifiers found in the literature. The first and most obvious observation is that none of the amplifiers is by far close to the 15 dB input

[1] Represented in this contract by CNIG, associated with the Instituto Geográfico Nacional (IGN) of Spain.

return loss in 100% of the band. Caltech LNA reaches this mark in 40% of its 15 GHz band. This illustrates how challenging is to match HEMT transistors in this frequency range. If we focus on noise temperature, the only amplifiers with less than 4 K on average have narrower bands than required. LNF LNA band, specified from 6 to 20 GHz, could be extended (with good noise) down to 4 GHz, achieving 16 GHz of bandwidth with around 4 K average noise. However, all these noise numbers are obtained for the optimum noise bias, with significantly more than the 9 mW of power permitted. The dissipated power could probably be reduced, but at the cost of an increased noise temperature and a reduced gain. Nonetheless, the most conflicting specifications are noise temperature and IRL. Any attempt to improve the input matching would affect the noise performance. Finally, note that even the required gain flatness of ±1 dB is only reached by one of the referenced amplifiers. In view of these data, it is quite obvious that the requirements of this study clearly surpass anything achieved so far.

Table 1: Performance of the best ultra-wideband cryogenic LNAs

Reference	Technology	Band (GHz)	(BW) (GHz)	T_{av}	(T_{min}) (K)	@T_{amb}	Gain (dB)	IRL %BW <10 dB	<15 dB	P_{dis} (mW)
[6] JPL 2006	100 nm InP	1-11	(10)	3.9	(2.3)	@4.1	31.5 ± 1.8	-	-	24
[7] CTH 2013	100 nm InP	0.5-13	(12.5)	4.4	(3.0)	@15	38.1 ± 2.9	64	0	15
[8] Caltech 2013	70 nm mGaAs	1-16	(15)	6.3	(4.5)	@21	36.9 ± 1.9	97	40	15
[9] CTH 2014	100 nm InP	6-20	(14)	5.8	(4.4)	@4	35.9 ± 0.8	70	37	13
[10] CTH 2018	100 nm InP	0.3-14	(13.7)	3.5	(2.2)	@4	41.6 ± 1.4	73	28	12
[11] CMT	70 nm mGaAs	1-18	(17)	6.3	(3.9)	@12	35.3 ±1.2	58	16	30
[12] LNF	100 nm InP	6-20	(14)	3.8	(2.5)	@5	32.8 ± 1.8	55	29	22

[7] and [8] share MMIC design with different transistors – [10] is commercially available (LNF)
[11] and [12] are commercially available versions of [8] and [9] respectively, optimized for a wider band [11] or using better devices [12]

Considering the mentioned "exploratory" character of this project, our approach to these "beyond the state-of-the-art" specifications, was on a best effort basis. It was clear for us from the beginning that a new generation of InP HEMT devices with improved performance had to be developed to get closer to the goals. The numerous transistor runs which had to be produced (and funded) to obtain the longed improvement, and the pandemic, were responsible for a two-year delay in completing the project. However, these efforts and the wait have paid off, as the final results exceed our initial expectations and are very close to the apparently unfeasible requirements.

1.3 Study Phases and Deliverables

The project contemplates five phases and seven work packages. A report was produced after each WP. Breadboard and prototype manufacturing data packages were included in the corresponding design reports. Two hardware deliveries were included at the end of the testing WPs. However, more hardware was built during the course of the project.

1. Review of foundry processes and development of breadboard LNA
    a. WP 1000: Review of foundry processes (**DRD 01** [13])
    b. WP 2000: Development of breadboard LNA design (**DRD 02**, **DRD 04** [3])
    c. WP 3000: Define measurement facilities (**DRD 03** [14])
2. WP 4000: Manufacturing, assembly, and testing of breadboard LNA (**DDR 05** [15], **D 01** Y420G 2001 amplifier)
3. WP 5000: Development of prototype LNA design (**DRD 06**, **DRD 07** [16])
4. WP 6000: Manufacturing, assembly, and testing of prototype LNA (**DRD 08** [17], **D 02** Y420G 3001 amplifier)
5. WP 7000: Final project evaluation (**DRD-09**, this report)

During phases 1 and 2 **two different single-ended design** approaches were modeled, manufactured and measured, not only one breadboard LNA as required by the SoW [2]. More additional tasks beyond what is described in the WPs, which we believe are of great interest for the project, were performed with two LNA units of one of the design versions:

- A 4-20 GHz cryogenic **balanced amplifier** was assembled and tested using these two LNAs and two **quadrature hybrid couplers** specifically developed for this purpose.
- The same **two LNA units were sent to NOVA** to be tested in their DSB and 2SB band-9 type receivers [18].

Figure 1: Amplifiers developed during the first two phases of the project. Y420G 2001 (baseline design and deliverable D 01) on the left. Y420G 1001 and 1002 (alternative design) on the center (sent to NOVA). Balanced amplifier (with 4-20 GHz hybrids) on the right.

The best of the these designs was chosen to be further developed in phase 3 of the project, producing the final amplifier. It is a hybrid design based on InP pseudomorphic HEMTs; the possibility of implementing a MMIC amplifier was discarded due to time constraints.

Apart from the final unit to be delivered to ESO, **three more units** of the same design were produced and tested in phase 4 of the project.

Figure 2: Amplifiers Y420G 3001, 3002, 3003 and 3004, designed, manufactured, and measured during phases 3 and 4 of the project. Only one unit was required by the SoW (final prototype Y420G 3001, deliverable D 02).

The TMP [1] does not fully reflect the effort dedicated to improving the existing transistors. This work was essential to the successful fulfillment of phase 4 and was extended during phases 1, 2 and 3, involving Diramics[2] for the manufacture of the devices and Yebes Observatory for the cryogenic

[2] Diramics is the Swiss foundry selected to produce the InP transistors for this contract. It is a spin-off from ETH-Zurich, which has been collaborating with Yebes in the development of InP HEMTs since the 90s.

characterization of its noise performance. Three experimental runs were needed, with only the first one covered by the financial support of this contract.

Finally, another transversal task of this project that did not finish after phase 1 and prolonged up to the final tests, was the upgrading of the measurement facilities.

1.4 ORGANIZATION

This report is divided in six sections, being the first this introduction in which we define the motivation and goals of the project comparing them with the state-of-the-art and describe the phases and work packages, pointing out the extra tasks done.

The second section summarizes the work done in collaboration with Diramics for the development of new and better transistors, starting with the aims of this development, the contents of the runs produced, the testing and modeling of the transistors in Diramics and Yebes and an outline of the many findings and achievements.

The third section is focused on the design and fabrication of the amplifier. Without going into too much detail, it overviews the decisions taken to define the type of design chosen and the selection and modeling of the most relevant components. Finally, it highlights the most important features of the final design and of the two previous designs.

The fourth section is dedicated to describing the measurement systems and procedures. As this was covered in a previous report, it emphasizes the singular cryogenic noise methods and systems and the improvements achieved in this project with the other measurement procedures.

The fifth section presents and discusses the results of the project, focusing on the final prototype developed. After exposing the measurement conditions and displaying a compliance / results table, several plots with new data of interest not included in the measurement reports are presented. Some of them are comparisons that highlight the good agreement with the model, the differences between the three designs, the similarities between units of the last design or the behavior under low power conditions. Other plots present new results, as the measurements of two 4-20 GHz LNAs in a sub-mm receiver, the performance of a new ultra-wide band LNA in the 2-18 GHz band or the results of a balanced amplifier in the 4-20 GHz band.

Finally, the last section draws some conclusions and recommendations for future lines of action to implement these amplifiers in the next generation of ALMA receivers.

2 TRANSISTOR DEVELOPMENT

2.1 AIMS

The requirements of this project were, as argued before, beyond what could be achieved with present technology. Given the importance of the transistors in the performance of a cryogenic amplifier, it was mandatory to develop a new generation of improved devices to have the possibility of getting close to the desired noise specifications.

The report about foundry evaluation [13] explains the advantages of HEMT transistors over HBTs and of InP over GaAs for this application and frequency range. Our partner for the development of InP HEMTs in this project has been **Diramics,** a Swiss spin-off company from the ETH with direct access to their clean room facilities. It was a logical choice, given that there was no other open and reliable source of InP devices in Europe (Chalmers University, being the only European alternative, is not so open to collaboration). We have a long and successful track record of collaboration with ETH and Diramics, and we have been supporting their cryogenic InP HEMT development line since the beginning 25 years ago.

The goals of this development were three:

- **Improvement of the stability of the devices**: Although this goal might not appear to be directly related with an improved performance, it should be noted that high frequency oscillations frequently affect a significant part of the Id-Vd bias plane, often preventing the devices from being biased at the optimum settings (or even at any useful bias). This is a historical problem of HEMT devices, aggravated at cryogenic temperatures. HEMT transistors are inherently unstable, and it is necessary to control the instabilities at microwave frequencies by a careful design of stabilizing networks. However, high frequency oscillations are intrinsic to the device and much more difficult to deal with. Diramics currently features 100 nm gate length technology which favors the stability and, in our experience, does not impair the noise temperature in this frequency range [19]. To further improve the stability, our approach was to change the layout of the transistors, modifying the metallization area, the number of fingers and the connection between fingers and contacts by air bridges.
- **Improvement of the minimum noise temperature of the devices**: This goal was addressed by changes in the material, namely, in the epitaxial structure and in the source to gate distance.
- **Reduction of the power dissipated at the optimum bias**: This was expected to be a consequence of the low noise optimization, as we will show later.

2.2 RUNS PROCESSED

Three experimental runs were processed during the project, the first of which was funded by ESO and the other two by Yebes.

- Run D181123-B (**1118**): This run tested a new source metallization area, various finger arrangements, and the implementation of different combinations of source, drain and gate air bridges. Two wafers were processed, in standard material and in a new material with a Schottky barrier around 25% thinner and with a modified epitaxial structure. An unknown problem during processing probably produced an excessive doping of the semiconductor. Consequently, the noise results with this material were degraded.

- Run D200629 (**0620**): The most successful topologies (source pad size, number of fingers and type of air bridges) tried in the previous run were included in this one to confirm the results. The material tested was the same as in run 1118 but with a Schottky barrier 50% thinner than the standard. This reduction was more aggressive than planned by design.
- Run D210406 (**0421**): This run sought only the optimization of the Schottky barrier, after some problems in previous runs. The layouts for each gate width were fixed. Two wafers called EPI1 and EPI2 with barrier height reductions of 15% and 30% respectively were processed.

Apart from the layout and material variations, each run included devices with different gate peripheries, from 50 to 400 µm. This was important not only because the amplifier to be designed would need transistors of different sizes in each stage, but also because with the information gathered from the measurements of different total gate widths, we could get a clearer picture of the device behavior.

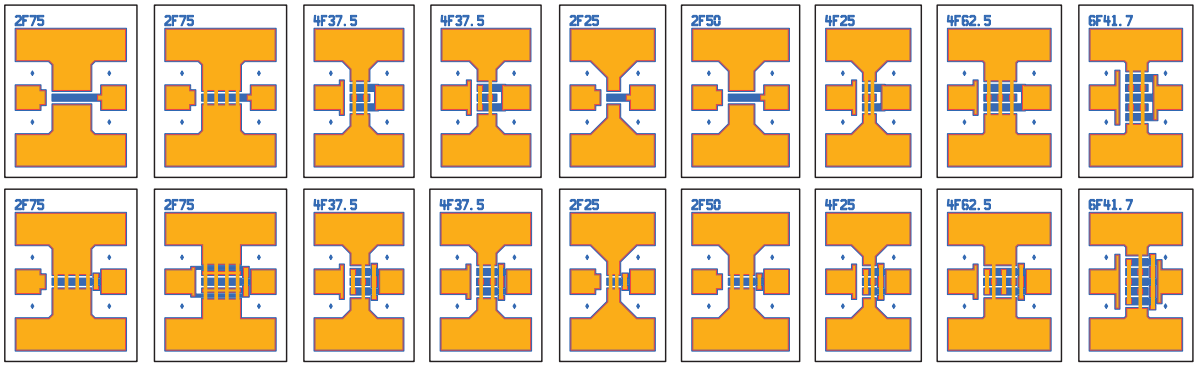

Figure 3: Examples of some of the topologies tested, changing the gate periphery, the number of fingers and the use of air bridges in source, drain and/or gate. Gate fingers are too small for this representation. They are placed at both sides of each blue drain contact. For each device, gate pad is on the left, drain pad on the right and source pads are at the top and bottom.

2.3 DEVICE TESTING

2.3.1 On-Wafer measurements

Diramics performs on-wafer **DC tests** of every single device delivered at room temperature and of selected devices at cryogenic temperature . The data obtained allows to discard bad devices, just by looking for example into the transconductance or the gate leakage.

Some parameters measured could be used even as predictors of device cryogenic performance. In particular, a reduction of the Schottky barrier height improves the control of the channel and provides higher transconductance for lower drain currents. This phenomenon can be quantified by a figure of merit defined as $\sqrt{I_d}/g_m$ that has been found to be correlated with the minimum noise temperature [20]. As shown in Figure 4, devices with lower figure of merit have better noise temperature, and both the lowest noise temperature and figure of merit are reached at lower drain currents for the best devices.

Other DC predictor of lower cryogenic noise is the subthreshold slope, that is, the speed at which the device turns on when increasing the gate voltage. Good devices have a sharper turn-on.

Diramics also performs on-wafer **scattering parameters measurements** of selected devices at room and cryogenic temperature and provide a small signal linear cryogenic model for a limited number of bias settings. Considering the number of transistor variants and bias, the number of models fitted is

enormous. From these measurements it is also possible to determine how prone is the device to oscillate.

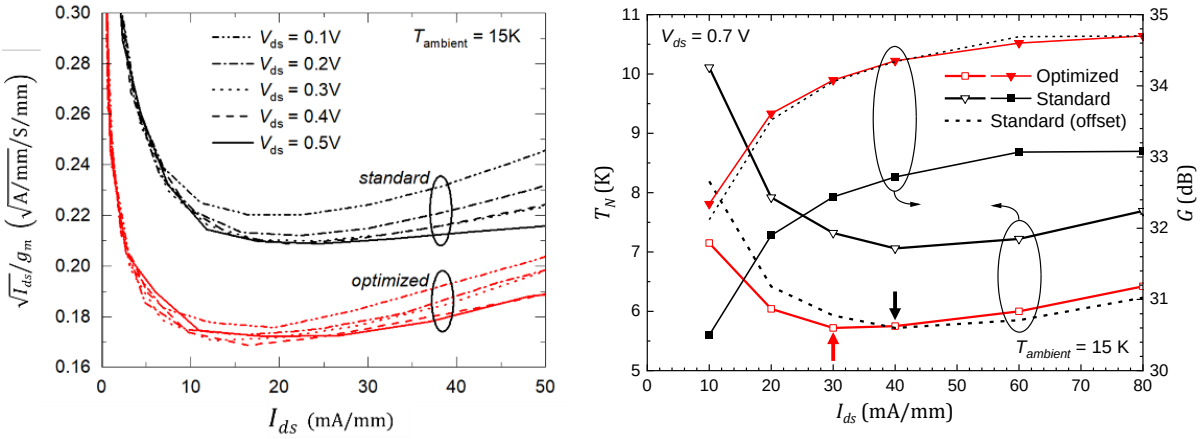

Figure 4: Comparison of the device figure-of-merit from cryogenic on-wafer measurements (left) and the average noise (thick lines) and gain (thin lines) of a test amplifier with the device in the 1st stage (right). Optimized devices in red exhibit better performance and a displacement of the minima to lower drain currents. Dashed lines in the plot on the right are normalized for easy comparison.

2.3.2 Device measurements on an LNA

Cryogenic noise parameters of the stand-alone transistors are extremely difficult to measure on-wafer with enough accuracy to be useful for LNA modeling. The **noise model** is obtained in Yebes from the noise measurements of the DUT in a test amplifier with a frequency band selected according to the DUT gate size. The parameters of the Pospieszalski noise model [21] are incorporated to the small signal model and calculated by fitting the measurements.

Using the same measurement system and amplifier, accurate comparisons between the performance of devices of the same size but different characteristics are possible (see for example, Figure 5 and Figure 6). The determination and comparison of the stable bias regions is also routinely done.

This process is very slow and demands a lot of time and effort.

2.4 Findings and Achievements

The following conclusions were drawn from the development and measurements of the transistors. They were applied to the selection of devices for the final amplifier.

- The reduction in source metallization area improves the stability by shifting to higher frequencies the resonance between the source pad parasitic capacitance (now smaller) and the bond wire inductance.
- The epitaxial structure (doping profiles) of the new material tested reduces impact ionization, contributing to a lower noise.
- Air bridges between gate and drain fingers help restoring the symmetry and avoid the odd-mode intrinsic oscillations that could appear otherwise, usually in topologies with wide (>100 µm) and numerous (four or more) fingers. However, it is better to avoid this solution for frequencies above X band, were the presence of these bridges (especially the gate ones) is detrimental to noise and gain.
- Two-finger devices are more symmetric and less prone to trigger these intrinsic high frequency oscillations. We did not measure a significant difference in noise performance with

multi-fingered devices; the higher gate resistance of the two-finger transistors is probably too low at cryogenic temperature to have a noticeable effect in noise temperature.

- Source air bridges have a more moderate – but always beneficial – effect enlarging the stable region of the transistors without a noise or gain penalty.
- A shorter gate to channel distance (Schottky barrier thickness) improves the channel control and ultimately, the minimum noise temperature, but a thinner barrier increases the gate leakage and consequently, the shot noise at low frequencies. The best compromise was found with a distance of 70% of that of the standard devices. Figure 5 compares the gain and noise performance achieved by devices with the different barriers tested in a 2-14 GHz amplifier.
- A decrease of the Schottky barrier thickness also increases the gate to source capacitance, which shifts the frequency response and can make matching of the transistor more challenging.

Finally, we have achieved the goals of this part of the study:

- We have obtained **stable devices** to be used in IF amplifiers. They feature two fingers, source bridges and reduced source metallization area. No instabilities were detected in on-wafer measurements and the whole measured bias regions (in the I_d-V_d plane) were clean when tested in an LNA.

- A **noise temperature improvement of around 20%** at 15 K for the EPI2 material of run 0421 with respect to the standard was measured in the first stage of the alternative 4-20 GHz design developed for this project (see Figure 6). This reduction was confirmed for transistors of different sizes tested in amplifiers from L to Q band.

- The noise temperature improvement is accompanied by a **reduction of the power dissipation**, as is typical of good devices. The optimized devices best bias is reached with a 25% lower current.

- A European firm, Diramics, has consolidated its role as supplier of state-of-the-art devices. Conversely to what happened with the first generation of ALMA LNAs, when European LNAs included US (HRL) devices, NRAO now has European devices from Diramics as first choice for its LNAs.

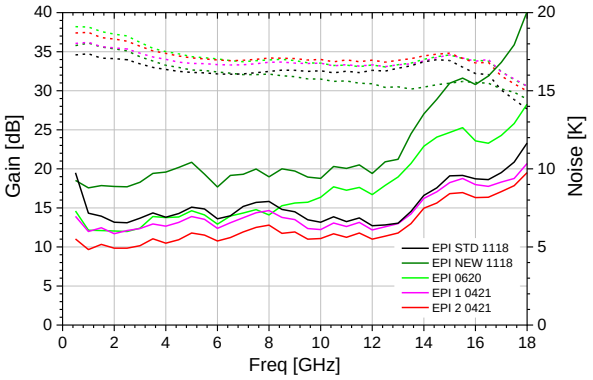

Figure 5: Comparison of the noise (solid lines) and gain (dashed lines) performance of different epitaxial materials of the three experimental transistor runs, measuring a test 2-14 GHz amplifier with the device under test in the first stage. Reference standard material of the first run 1118 in black. In dark green, the flawed new epi of the same run. Run 0620, with an excessively thin Schottky barrier is in light green. The last run 0421 featured Schottky barriers between 1118 and 0620, being the thinner EPI2 (in red) the one with the best noise results.

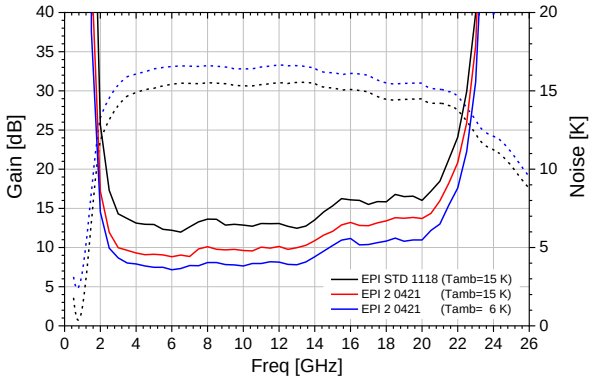

Figure 6: Measurements of the impact of the new transistor mounted in the first stage of amplifier Y420G 1001 (alternative design of the 4-20 GHz amplifier [15]). Noise curve in black corresponds to the original version at 15 K (average noise 7 K). Red and blue curves use the new device from Diramics 0421 EPI2 in stage 1 at 15 K (average noise 5.4 K) and at 6 K (average noise 4.4 K) respectively. Gain curves use the same colors (dashed lines). Difference in gain is due to the transistor change but also to an adjustment of the source feedback needed to tune the new transistor.

3 AMPLIFIER DESIGN AND FABRICATION

3.1 DESIGN CHOICES

Before starting the design itself, some decisions must be taken about the basic characteristics of the amplifier. Most of them are explained in depth in [3]. Follows a summary of these choices:

- **Band selection**: The specifications leave open the placing of the required 16 GHz band in the 0.1-24 GHz frequency range. The 4-20 GHz band is a compromise between low noise and good matching based on actual results of cryogenic InP HEMT LNAs. As the band is shifted higher in frequency, the minimum noise temperature (which has a roughly linear dependence on frequency) increases and deviates from the noise specification. If the low end of the band is shifted too low in frequency, the fractional bandwidth becomes excessive and the matching of InP transistors becomes impossible or requires serious trade-offs in noise and gain flatness.

- **Technology selection**: The amplifier is designed in hybrid or “chip&wire” technology (also known as MIC). MMIC technology was considered as an option but discarded early in the project given the time constraints and the insufficient maturity level of this technology at Diramics. Nevertheless, MIC technology offers obvious advantages for fast prototyping, features lower loss of the matching circuits and permits the use of transistors of different materials in each stage. These benefits were all exploited in this design. The choice of transistor technology has been treated in the previous section.

- **Number of stages**: The design has three stages. This is just enough to reach the gain requirement of 33 dB with these transistors at 20 GHz. More stages would give more degrees of freedom to equalize the gain or optimize the output matching but would increase the power dissipation.

- **Biasing scheme**: The amplifier has independent bias lines for each stage. This is very important in a prototype to be able to optimize each stage bias separately and to pinpoint problems more easily.
- **Topology**: The classical common source topology is used in all stages, as is typical of low noise amplifiers. The transmission lines of the matching circuits are implemented in microstrip, very convenient to interface with lumped elements by means of bond wires.

This kind of amplifiers have demonstrated high reliability and are currently in use in ALMA bands 5, 7 and 9.

3.2 Components and Devices Selection and Modeling

In the same way that a MMIC designer has a "Product Design Kit" with models and design rules for each available design element, in a MIC design such as this, the designer must build its own library of models for all suitable components, microstrip lines and bond wires. This is especially important and difficult in a cryogenic application, where no supplier gives any data, and each component must be validated and tested through a slow and complicated process.

An important part of the design effort was directed to this selection and modeling task, which is described in project reports [13], [3] and [16] and in Yebes Observatory reports [22], [23] and [24]. Follows a summary of the works done and the most significant advances in this phase of the project.

3.2.1 Transistors

Transistor modeling was covered in section 2.3. Three key aspects in the selection of transistors contributed to the success of the design:

- Selection of devices with the right topology (two fingers, source air bridges, reduced pads), with no oscillation problems. This is a consequence of the transistor development phase and has saved a lot of time during the tuning phase (it can save a whole design!) and improved the overall performance of the amplifier.
- Selection of devices with the right size: In an ultra-wide band LNA, this step is of outmost importance and will condition the rest of the design. In general, as the gate width shortens the matching of a transistor improves for higher frequencies. However, for a low noise amplifier like this there are several conflicting criteria involved in the gate width selection [3], namely: (a) equilibrium between low (wide gate) and high (narrow gate) frequency noise matching due to the variation of the optimum noise resistance, (b) gain roll-off compensation at high frequency (narrow) (c) low power dissipation (narrow). These criteria weight differently for each stage and were tweaked by modeling and dedicated measurements. Accordingly, the selected sizes were 200, 150 and 100 µm for stages 1, 2 and 3, respectively.
- Possibility of using devices from different runs (epitaxial materials) in each stage: We have already commented on this advantage of MIC designs. In this case we use devices from run 0811 (standard material) in stages 2 and 3 and a device from run 0421 EPI2 (best noise material) in stage 1. The lower Cgs of the standard Schottky barrier helps to compensate for the higher gain roll-off of the first stage. The higher noise contribution of 0811 transistors is negligible in stages 2 and 3.

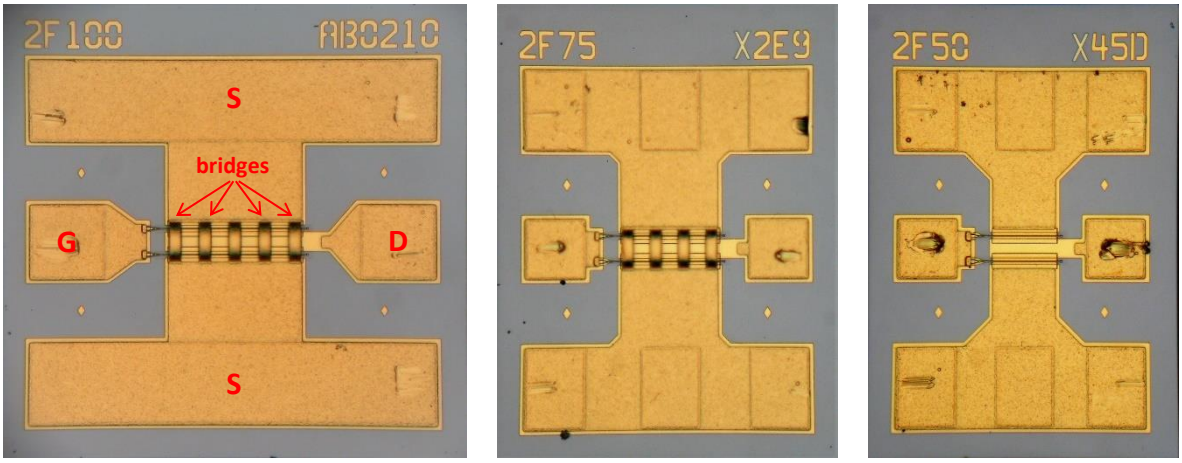

Figure 7: Photographs of the transistors selected for stages 1, 2 and 3 (from left to right) of the amplifier. They are all 2 finger devices with total widths of 200, 150 and 100 µm, respectively. All cryogenic models were available. Note the source air bridges of the first and second transistors. The first transistor comes from the final run with the new EPI 2 material. It presents also slightly larger pad areas to prevent damage to gate fingers and air bridges during the bonding process.

3.2.2 Inductors

This design introduced the use of chip spiral inductors on quartz substrate in our MIC LNAs. Some manufacturers are now offering inductance values in a sufficiently small size and with a high enough self-resonance frequency to be used in the matching and bias circuits.

As this was a new component, an assortment of values, types, and sizes from three different suppliers were tested in our coplanar probe station. The multiple equivalent circuits obtained fitting the measured S parameters [23] were used in the amplifier model to select the best option (usually the one with the lowest parallel parasitic capacitance for the required inductance).

Three functions are played by these inductors:

- They can advantageously substitute the big resistors or conical inductors traditionally used to introduce the first stage gate bias without impairing noise. An average noise temperature improvement of 1 K was measured in the alternative design when changing to a spiral inductor.
- They can be implemented in the drain bias lines to realize the inductance needed instead of long bond wires, adding flexibility to the tuning.
- They are placed in parallel with drain resistors, nulling the dissipated power, and allowing higher resistance values to be used.

3.2.3 Resistors

Another novelty applied to the present design was the use of 0102 (0.25×0.5 mm) NiCr thin film resistors on quartz substrate. The lower dielectric constant of quartz and their smaller die size reduces the resistor's parasitic capacitance to ground, improving the frequency response. A selection of values in the range to be used were measured in our coplanar probe station and a simple parametric model with the same parasitics for all resistances was defined [22].

However, the relatively low thermal conductivity of fused quartz and the very small size reduce the power handling capacity of these components. This problem had to be analyzed because some of them support currents of several mA, as needed to bias the wide gate first stage transistors. The self-heating effect could increase the thermal noise and degrade the performance of the amplifier. A study was conducted [24] to model the temperature rise of the resistors and rule out this possibility.

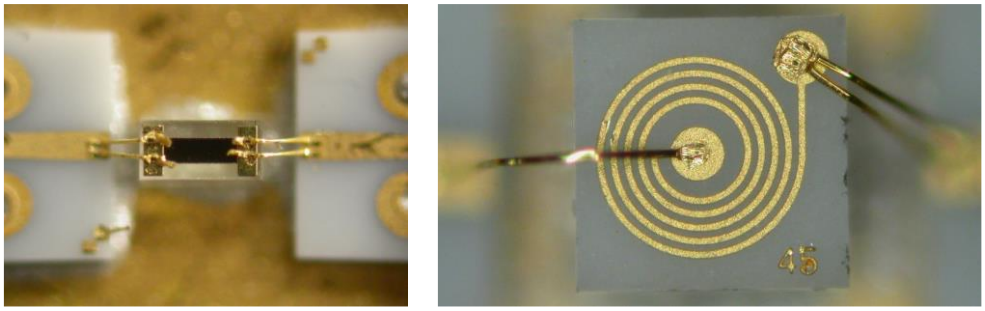

Figure 8: Photographs (not to scale) of a quartz thin film resistor (left) and a quartz spiral inductor (right) placed in the test fixture used for the characterization with the coplanar probe station. The chips have the same length of 0.5 mm.

3.2.4 Other circuit elements

- All **capacitors** (except the 10 nF CG0 used as charge divider at the bias inputs) were MIS type chips, on silicon substrate with SiO2 dielectric. They are nearly ideal for this frequency range and no equivalent circuits were needed. However, the DC blocking capacitors are critical for gain equalization; the specific configuration of two serial capacitors used to achieve the very low capacitance needed was modeled with electromagnetic CAD software and measured in a test fixture.

- **Bond wires** are very sensitive elements of the circuit. The transistor or DC capacitor bond wires are actual design tools, and useful tuning elements. Special care was taken in the modeling. Long bond wires are modeled after long high impedance transmission lines to account for the distributed effects of the inductance (the impedance depends on the particular bond wire realization). Short ones are modeled as simple inductances and translated into geometric parameters considering the ADS NXP bond wire model and experimental measurements.

- **Transmission lines** are represented according to the traditional Libra-ADS models.

3.3 Design Highlights

3.3.1 Final prototype design

For a complete description of the final design, consult the design reports [3]. Some significant design features and achievements are listed below:

- The introduction of **new and better components** (spiral inductors, small quartz resistors) reduced the parasitics allowing an improvement of the frequency response at the band edges and of the noise penalty in the first stage (see previous section).

- The **bias circuit design** has been improved. On the one hand, it is simpler, featuring now one RC filtering section less but keeping similar effectiveness separating the microwave signal from the DC bias. On the other hand, it dissipates less power, thanks to this simplification and the use of the bypass inductors in parallel with the drain resistors. An ESD protection level complying with the specifications is still realized by a 10 nF capacitor and two antiparallel Schottky diodes.

- **Unconditional stability** is intentionally reached by a low margin as most of the stabilization mechanisms operate against performance. Drain resistive loading and inductive source degeneration are two classical methods used.
- The **input matching network** is simple, to avoid restricting band. The matching is dominated by the gate size dependent transistor input impedance. It is optimized for the high frequency end and degenerates with decreasing frequency. The admittance is matched by a long bond wire. A short low impedance line that acts as a small capacitance, responsible for a long ripple in the noise response that widens the noise band.
- It is difficult in such a wide band amplifier to separate the effects of each circuit elements, as most of them influence many design goals. To achieve a good **gain equalization**, besides other methods like the aforementioned resistive loading, this design relies mainly on the DC blocking interstage capacitors and bond wires, enhanced at the high frequency end by inductive peaking.
- An intensive **use of simulation tools** (ADS) was needed to reach the tight results achieved, especially in the band edges. Many iterative optimization cycles assigning weights to different circuit sections and involving different goals were performed.
- Microstrip circuits are laser-etched and cut in a soft Duroid 6002 substrate with low dielectric constant and excellent thermal properties. The low thickness (5 mil) allows for a compact arrangement of the lumped components (with short bond wires) critical for this design.
- No changes were made for these amplifiers in the assembly and interconnection techniques used in our labs, with proven in the field reliability.

A simplified schematic of the design, showing the components used is shown in Figure 9. No transmission lines or bond wires are represented.

Figure 10 and Figure 11 illustrate the appearance of a disassembled and an assembled unit. The first one is a simplified 3D rendering of an exploded view and the second, a photograph of an amplifier without cover, exposing the microwave cavity and bias circuitry.

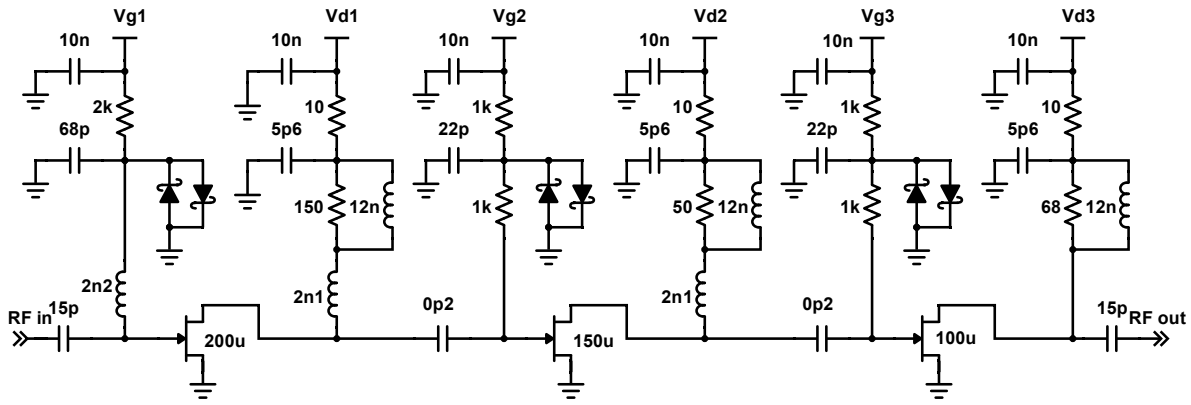

Figure 9: Simplified schematic of the three stage 4-20 GHz final LNA design. Only discrete components are represented (no microstrip lines or bond wires). A complete schematic is given in [16].

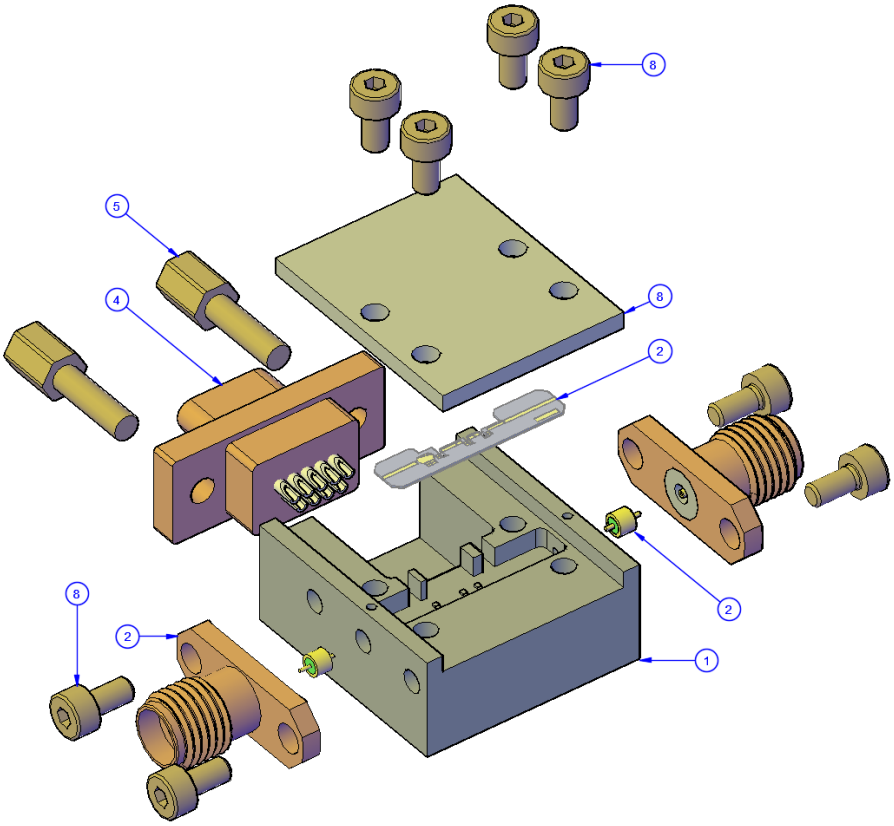

Figure 10: Exploded view of the final LNA, showing all its major parts. Chip components not shown.

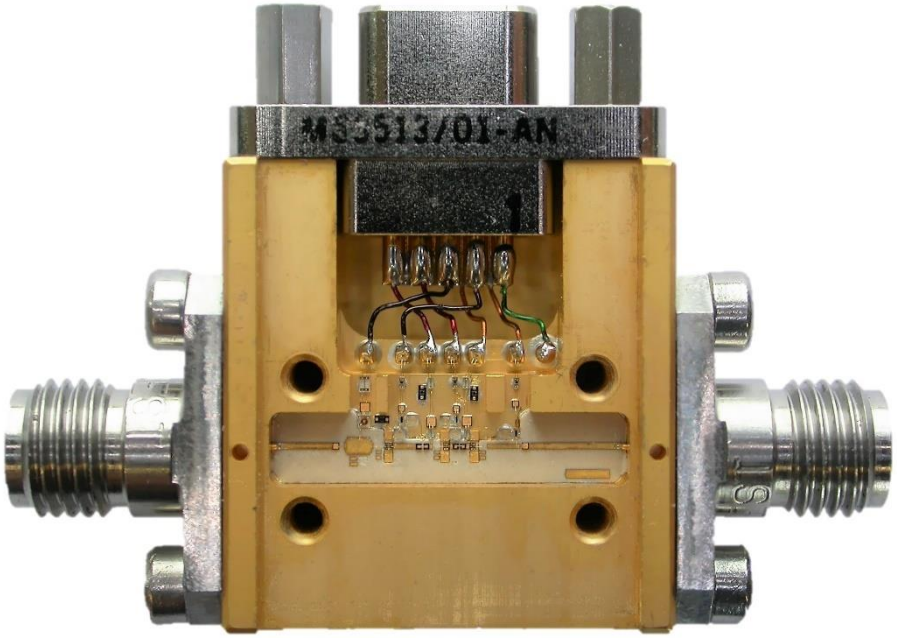

Figure 11: Inside view of the manufactured unit Y420G 3001. The left 2.92 mm connector is the and the right one is the output. The top MDM connector is used to introduce the bias. Dimensions excluding connectors are 20×22×9 mm.

3.3.2 Other designs

A description of the **breadboard baseline design** can be found in [3] and Appendix A of [15]. This amplifier is a deliverable of the project (D 01). The main differences with respect to the final prototype are listed below:

- The lack of some transistor models (for certain types and bias settings) in the initial phase of the project forced the use of scaled or extrapolated models. This led to worse model predictions.
- The optimized transistor batch was not available to be used in the first stage.
- The assortment of chip inductors was limited and there were only theoretical models available at the time of the design. This limited its use and conduced to worse model predictions.
- The use of quartz resistors was possible only in the measurement and tuning phase. The design was done counting with the higher parasitics of alumina resistors, and this affected the performance even after the replacement of some of them.
- The bias lines scheme used one more filtering section and different drain resistors and capacitors. The power dissipated in the drain lines is higher. Only one bypass inductor (in the first stage) is used.
- Due to an error in the circuit layout, the output reflection measured results were poor. Even though this error was partly compensated in the assembled unit, the reflection was still worse than designed.

A description of **the breadboard alternative design** can be found in Appendix 1 of [3] and Appendix B of [15]. Two units of this design were used in a balanced amplifier and later sent to NOVA. This is a simpler design developed in the first phase of the project as a less risky solution. It avoided the main sources of uncertainties at that stage when no data was still available about some components and transistor types. Moreover, the optimization goals were relaxed, yielding an amplifier more likely to perform as designed. The main differences with respect to the breadboard design are:

- Simpler input matching network.
- Identical second and third stages matching and bias circuits.
- No spiral chip inductors used in the design. A broadband conical inductor was implemented to bias the first stage gate. It was later replaced in the assembled units by a chip inductor with great advantage. Long bond wires were used in some bias lines to achieve medium value inductances.
- No small-size low-parasitics quartz resistors used in the design. The last-stage alumina 0302 resistor was later replaced in the assembled units by a quartz resistor significantly improving the output reflection.
- Last stage transistor width was 150 µm.
- No fine-tuning attempted by tweaking bond wire inductances in transistors and DC capacitors.

4 MEASUREMENT SYSTEM AND TEST PROCEDURES

4.1 NOISE MEASUREMENTS PROCEDURES AND ACCURACY

A critical task in the development of cryogenic low noise amplifiers is to stablish accurate, precise, and reliable measurement methods. This is especially true in the case of noise temperature characterization, where the measurement uncertainty is often comparable to the noise magnitude, and the results of different laboratories can differ notably.

To increase confidence in results given we have used **two independent methods** to determine the noise temperature of the amplifiers: the cold attenuator method (CA) and the variable temperature cryogenic load method (VTCL). The first one is based on an external diode noise source connected to a cryogenic attenuator at the input of the DUT, which can be controlled by commercial noise figure measurement equipment. It is very convenient for optimizing the LNA, as the data acquisition is very fast, but the accuracy depends on a complex calibration. The second method (VTCL) relies on a matched load cooled to a controlled cryogenic temperature and connected to the input of the DUT. It was used for the final measurements because it provides higher accuracy, but the process of temperature stabilization between hot and cold measurements makes it slower. More details are given in [14].

The data obtained by both procedures are completely independent, as each one was implemented in a different setup (different dewar and measurement equipment), as described in [14]. Photographs of both systems, based on a CTI and a Sumitomo refrigerator, respectively, are shown in Figure 12. The estimated **measurement accuracy** calculated by Montecarlo simulation with a coverage factor of 2 [25] for an LNA of the characteristics (noise and scattering parameters) of this one at an ambient temperature of 15 K is ±1.2 K for the setup using the CA method and ±0.7 K for the setup using the VTCL method. Note that the repeatability of the measurements of each system is much better (of the order of ±0.1 K), which allows accurate comparisons between different amplifiers.

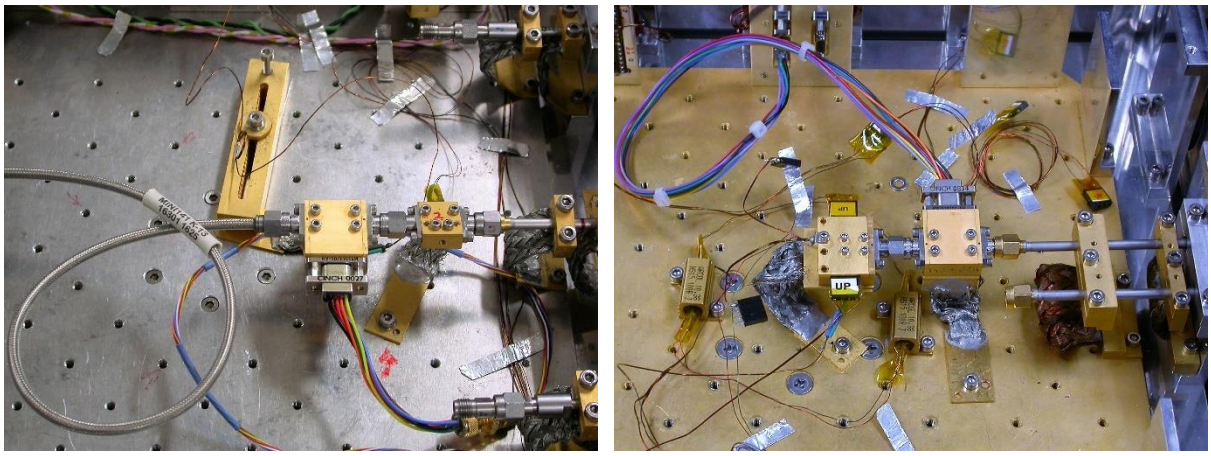

Figure 12: LNA noise measurements using two different setups and methods. On the left, the CA in system 1020-3. On the right, the VTLC in system SUMI-1. Ambient temperature of system SUMI-1 can be controlled down to 5 K, while system 1020-3 only cools down to 15 K.

A comparison between the measurements in the VTCL system and the CA system is presented in Figure 13. An LNA of the final design was tested at 15 K[3] using both methods. The average noise temperature difference is around 0.5 K, well inside the error bars defined previously. The dotted blue trace corresponds to the VTCL measurements at 5.5 K, and it is represented here as a reference for the noise data presented in this report. Note that the noise temperature improves 1.2 K between 15 K and 5.5 K ambient temperature.

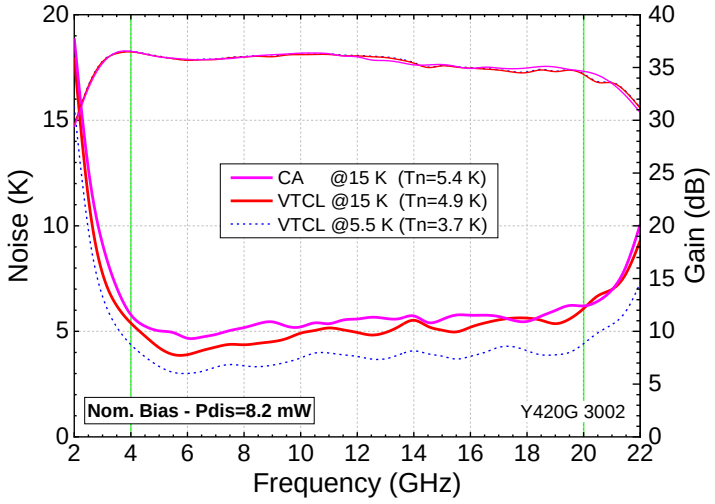

Figure 13: Comparison of the cryogenic noise temperature and gain of LNA Y420G 3002 at 15 K ambient temperature measured in system SUMI-1 with the VTCL method and in system 1020-3 with the CA method. The additional dotted line shows the results with the VTCL at 5.5 K ambient. Nominal bias settings in Table 2.

4.2 Cryogenic Tests Systems Developments

Reports [14], [15] and [17] describe some of the **upgrades of the noise measurement system** (CA) completed along this study to adapt it to the requirements of the project and to improve the accuracy of the results. We summarize them shortly here:

- Extension of frequency range from 0-20 GHz to 0-26.5 GHz.
- Recalibration of Agilent and Keysight diode noise sources utilizing a method developed using the Keysight PNA-X noise receiver [26]. Some inconsistencies were found in the manufacturer calibration tables and we believe that the new ENR is more accurate.
- Substitution of the commercial stainless-steel coaxial line used as a thermal break at the input of the dewar by a new stainless-steel air-line crafted in-house to reduce the uncertainties associated with inner dielectric displacements due to thermal cycling.

4.3 Other Measurements

Most of the procedures to measure the other electrical parameters (scattering parameters, stability, gain fluctuations, linearity, and phase time-variations) follow what is described in the Definition of the

[3] Note that the system with a CTI refrigerator, implementing the CA method, is only capable of cooling down to around this temperature, while the system used for VTCL measurements, with a Sumitomo refrigerator is capable of controlling the ambient temperature in a wide range down to 5 K.

Measurement Procedures report [14]. Some **extra procedures** were introduced to test the final amplifier, as explained in [17] and outlined below:

- Stability: To ensure the absence of oscillations, besides calculating the Rollet factor, the cryogenic DC curves (Id-Vd) of each stage were analyzed with the amplifier connected to the VNA and loaded with shorts.
- Gain fluctuations: To improve the quality of the gain fluctuations measurements for the shortest period Allan variance required (where the fluctuations of the VNA of the "standard" setup are close to the specs), an alternative setup including and FFT analyzer was used. The results of both systems are presented together to cover the whole Fourier frequency range.

Finally, this project required other measurements to characterize components (using coplanar probe station and test fixtures to cool down the DUT) and transistors (with Diramics cryogenic probe station and Yebes procedure to measure the Pospieszalski cryogenic noise parameters). They have been already described in previous sections of this report.

5 AMPLIFIER RESULTS AND ANALYSIS

The complete results of the amplifiers to be delivered are presented in [15] and [17]. The following sections present a compliance matrix including a summary of the results of the final unit, and new plots with data comparisons providing some insight about the agreement with the models and the difference in performance of the different designs. Finally, other plots present new information obtained after the completion of phase 4 of the project, which we think is very relevant for the possibility of implementing an amplifier of this kind in a future ALMA receiver.

5.1 AMPLIFIER TEST CONDITIONS

5.1.1 Ambient temperature

The technical specifications [8] do not define a fixed temperature for the tests, but just a temperature range from 2 to 18 K. Most specified parameters are quite insensitive to temperature changes across this range and were measured at 15 K for convenience (it is the nominal temperature of an amplifier in our IF amplifiers Dewar, system 1020-3). However, noise temperature does depend significantly on ambient temperature. In our amplifier this variation was found to be 0.12 K of noise per K of temperature. For this reason, we performed the noise tests for all biases in our controlled temperature Dewar with the VTCL (system SUMI-1) at two temperatures, 5 K (the lowest possible) and 15 K (to compare with the other system which uses the CA method). It is not clear if the noise specifications apply to the highest possible ambient temperature of 18 K.

We will only provide in most of the following sections results at an ambient temperature of 15 K (for most electrical parameters) and at 5 K (for noise). For room temperature data, noise results at 15 K, or noise and gain dependence with temperature, refer to [15] and [17].

5.1.2 Bias

Table 2 provides the bias settings used in the measurements of the final design units. Bias #1 is referred to as nominal and is considered the best compromise for optimized performance.

The results of LNA Y420G 3001 as presented in [17], in Table 3 and in Figure 14 and Figure 15 are also given for another bias (#2) with a slightly reduced power dissipation and negligible variation in performance.

The voltages given in the table are measured at the DC power supply terminals. The resistance of the bias lines of our system (4 Ω) produces a small drain voltage drop and a dissipated power which strictly should not be accounted for in the LNA budget (around 0.7 mW for the typical nominal bias). The values given in this report do not take this into consideration.

Table 2: Bias settings used in the measurements presented in this report. Bias #1 is referred to as nominal. Y420G 3001 is the unit delivered to ESO (D 02)

Y420G 3	**Stage 1**			**Stage 2**			**Stage 3**		
Gate width	200 µm			150 µm			100 µm		
Drain DC resistance	10 Ω			10 Ω			10 Ω		
	V_d (V)	**I_d (mA)**	**V_g (V)**	**V_d (V)**	**I_d (mA)**	**V_g (V)**	**V_d (V)**	**I_d (mA)**	**V_g (V)**
Room temp. bias	0.70	12.0	0.19	0.55	9.0	0.01	0.70	6.0	-0.02
#3001 Bias #1 (8.2 mW)	0.70	6.0	0.21	0.45	4.5	0.06	0.65	3.0	0.02
#3001 Bias #2 (6.5 mW)	0.65	5.0	0.21	0.40	4.0	0.06	0.55	3.0	0.03
#3002 Bias #1 (8.2 mW)	0.7	6.0	0.21	0.45	4.5	0.05	0.65	3.0	0.02
#3003 Bias #1 (8.5 mW)	0.7	6.0	0.20	0.5	5.0	0.04	0.60	3.0	0.02
#3004 Bias #1 (7.9 mW)	0.65	6.0	0.21	0.5	5.0	0.05	0.50	3.0	0.04
#3004 Bias #2 (4.6 mW)	0.50	4.0	0.21	0.40	4.0	0.05	0.40	2.5	0.04
#3004 Bias #3 (2.8 mW)	0.50	3.0	0.21	0.30	2.50	0.04	0.30	2.0	0.04

5.2 Performance and Compliance of the Delivered unit Y420G 3001

The results of the final prototype are presented in [17]. For the sake of completeness, we include two tables with a summary of the results and the compliance of the final prototype (unit Y420G 3001) with the requirements in [4].

Table 3 displays the electrical specifications and performance, while Table 4 lists the environmental, interface and RAMs requirements met by design. The degree of compliance is indicated by fA (fully accomplished), pA (partially accomplished) and nA (not accomplished).

Table 3: Performance of amplifier Y420G 3001 at the bias settings of Table 2 and compliance matrix of the electrical specifications. Unless otherwise noted, measurements were taken at 15 K and correspond to the 4-20 GHz nominal band of the LNA. Parameter number is the suffix from the specification code number FEND-40.02.00.00-02XXX in [4].

Parameter [4]	**Measurement**	**Results**		**Specification** [4] **and units**	**Compliance**
		Bias #1	**Bias #2**		
#190 **Power dissipation**	*DC consumption*	8.2	6.5	< 9 mW	fA
#180 **Noise temperature**	*Average @5 K*	3.7	3.8	< 4 K	pA Complies average noise temp. @5 K
	Maximum @5 K	4.4	4.6		
	Average @15 K	4.9	5.0		
	Maximum @15 K	5.8	5.9		
#110 **Gain**	*Average*	35.5	34.7	33<$\|S21\|^2$ $\|S21\|^2$<41 dB	fA
#120 **Gain flatness**	*Max. excursion*	1.8	1.7	<2 dBpp	fA
#090 **Input reflection**	*Maximum*	-11.8	-11.4	$\|S11\|^2$<-15 dB	pA Complies 97% of the band
	Max. 95% of the band	-15.1	-14.3		
#100 **Output reflection**	*Maximum*	-15.3	-14.7	$\|S22\|^2$<-15 dB	fA
	Max. 95% of the band	-15.9	-15.1		
#170 **Stability**	*Minimum Rollet factor*	2.0	2.0	K> 1	fA
#130 **Gain compression**	*P1dB @4 GHz*	-9.3	-9.4	>-10 dB	fA
#150 **Gain variation with temperature**	*Average in the band*	$7.3\cdot10^{-3}$		<0.05 dB/K	fA
#140 **Gain fluctuations**	*Max. $\sigma^2(\tau)$ 0.05≤τ≤100 s*	$1.5\cdot10^{-8}$	$1.1\cdot10^{-8}$	$<2\cdot10^{-8}$	fA Tested @12 GHz only
	(Allan var) 100≤τ≤300 s	$6.5\cdot10^{-8}$	$6.5\cdot10^{-8}$	$<2\cdot10^{-7}$	
	SNGF @ 1Hz ($Hz^{-½}$)	$7.7\cdot10^{-5}$	$9.1\cdot10^{-5}$	-	
#160 **Phase variation with time**	*Φ_{S21} peak dev. in 5 min.*	0.07	0.08	<0.5°	fA

Table 4: Compliance matrix of interfaces, environmental requirements and RAMS met by design. Parameter number is the suffix from the specification code number FEND-40.02.00.00-02XXX in [4].

Parameter [4]	Specification [4]	Compliance	
#080 **Frequency range**	>16 GHz in (0.1,20) GHz	fA	Electrical specifications measured in 4-20 GHz band
#030 **Operating temperature range**	2 K - 18 K	pA	The LNA design and test temperatures are 5 and 15 K. Noise and gain have also been tested at several temperatures in the 5-18 K range. The other specs do not change significantly with temperature.
#020 **Temperature cycling**	Withstand >100 cycles RT to 4 K	fA	Tests made for ALMA IF LNAs of bands 5, 7 and 9 with similar technology. Prototype amplifier cycled around 20 times.
#010 **Outgassing**	ALMA System: Electro-magnetic Compatibility (EMC) Requirements	fA	This design does not include any component or chemical with outgassing risks other than the ones used in ALMA IF LNAs of band 5, 7 and 9, compliant with this requirement.
#050 **ESD**	Level 1 ESD Requirements according to [27]	fA	Implemented ESD gate protection circuits designed to withstand level 1 conditions as described in [16]. No tests have been made to guarantee compliance with ALMA requirements.
#060, #070 **RF interfaces**	50 Ω Female SMA	fA	Field-replaceable SMA compatible 2.9 mm female connectors, with glass beads integrated in the amplifier chassis. Better high frequency matching than standard SMA.
#200 **Lifetime**	> 15 years	fA	None of the processes or components used have declared limits in its lifetime. No signs of degradation have been observed in hundreds of similar amplifiers manufactured by our institution in more than 30 years.
#210 **MTBF**	> 128 years	fA	The MTBF estimated from the field data available from similar amplifiers delivered to ALMA and NOEMA (an overall time of operation of ≈9000 years) is 680 years.
#220 **Maintenance**	No periodic maintenance	fA	No maintenance is needed

5.3 Comparison with Modeled Results

The final results in gain, noise and reflection for two different bias are presented in Figure 14 and Figure 15 compared with the modeled predictions. The agreement is quite remarkable and gives value to the great effort put in the cryogenic modeling of all the elements of the amplifier.

The model used in the design and presented in [16] did not include the coaxial connectors and beads, but the measurement planes are referred to these connectors. The curves of these plots were calculated incorporating a connector model, hence the difference with the originals and the better fitting of the reflection plots.

The difference in average gain could be partly due to the small bias differences between the transistor models and the actual bias applied in the amplifiers. Note that cryogenic transistor models are not parametric and only a very limited set of bias settings were measured. After bias optimization, the original bias of the model differs from the bias used in the measurements.

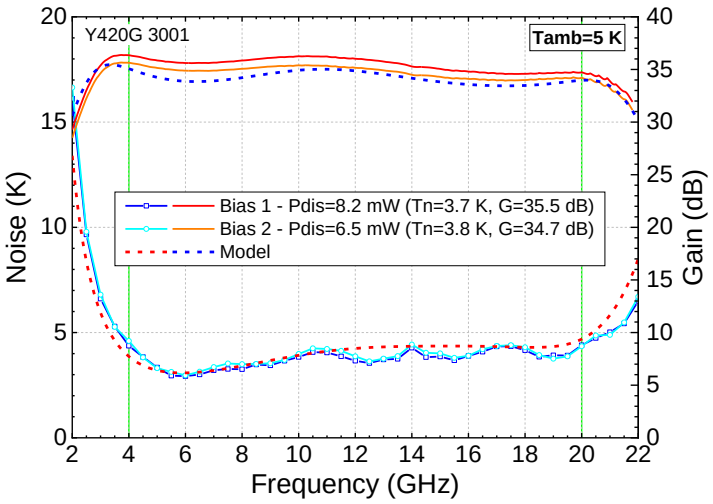

Figure 14: Cryogenic noise and gain results of the delivered unit, final prototype amplifier Y420G 3001, at two bias settings (see Table 2), compared with the model (dashed lines).

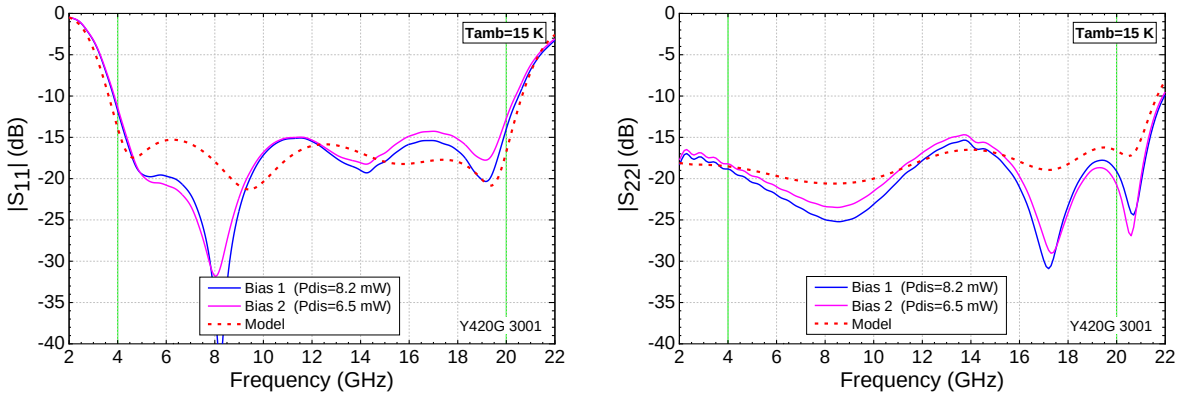

Figure 15: Cryogenic input and output reflection of the delivered unit, final prototype amplifier Y420G 3001, at two bias settings (see Table 2), compared with the model (dashed lines).

5.4 Comparison Between Different Designs

Figure 16 and Figure 17 compare the noise, gain and reflection results of the three designs described in section 3.3: the final prototype design, the breadboard baseline design and the breadboard alternative design.

The differences in gain owe mainly to the different equalization techniques and the more conservative values of the DC blocking capacitors in the alternative design. The noise improvement of the final design is due to the use of an optimized transistor in the first stage, while the differences with the alternative design are related with the simpler input matching and less ambitious optimization.

Input reflection of the alternative design at low frequency was not prioritized, hence the poor results. The high output reflection of the baseline design is a consequence of a layout error. The final design reflection results profits from the availability of a wider range of small quartz inductors and resistors and of an a priori optimization with good models.

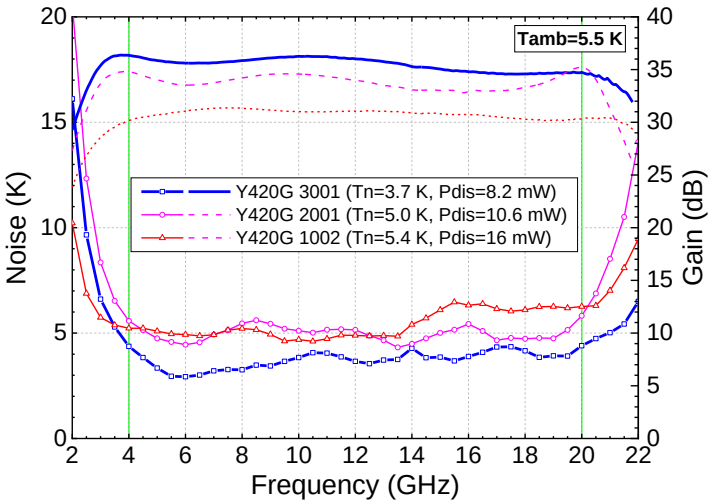

Figure 16: Comparison of the cryogenic noise temperature and gain of the breadboard LNAs 1002 (alternative design) and 2001 (baseline design) and of the final prototype 3001. Bias settings are nominal for the three units.

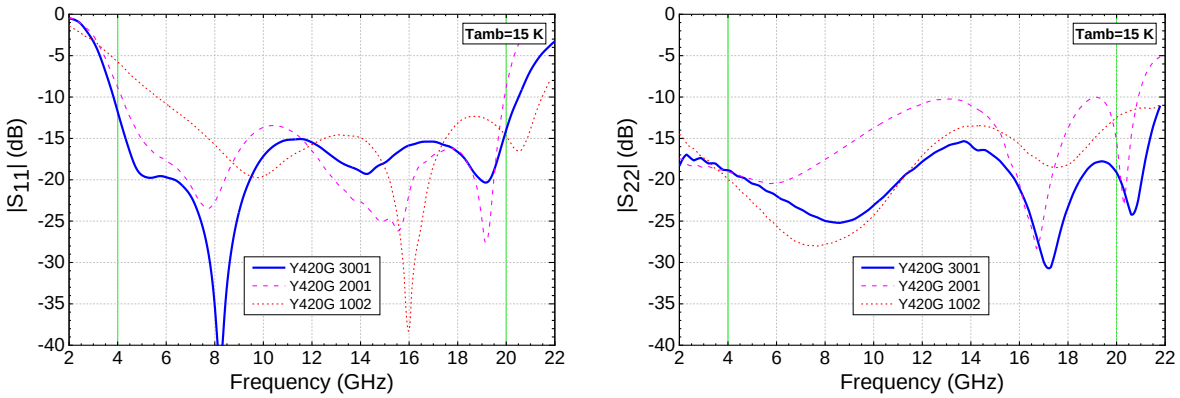

Figure 17: Comparison of the cryogenic input and output reflection of the breadboard LNAs 1002 (alternative design) and 2001 (baseline design) and of the final prototype 3001. Bias settings are nominal for the three units.

5.5 Repeatability of the Results in Four LNAs

Three additional units of the final design were assembled and measured. It is significative that the adjustments needed to achieve the measured results were minimal.

Figure 18 and Figure 19 show the gain, noise and reflection results of the four LNAs. The remarkable similarity of the curves support that the amplifiers are quite repeatable. Amplifier Y420G 3003 suffered an issue during the assembly (slightly incorrect placement of the microstrip substrate) that produced a little deviation in the performance (input matching) with respect to the other units.

Gain fluctuations were not measured for all units. The remaining electrical parameters (not shown here) of the three units are also extremely similar to Y420G 3001.

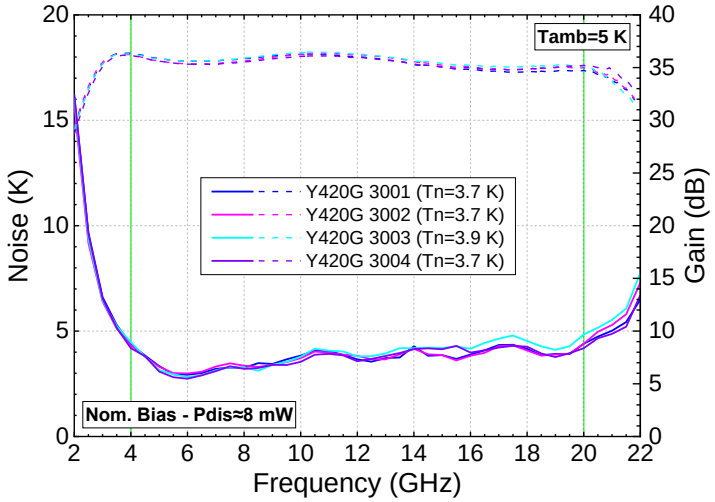

Figure 18: Comparison of the cryogenic noise temperature and gain of the four manufactured units of the final design. Bias settings are nominal (#1 in Table 2).

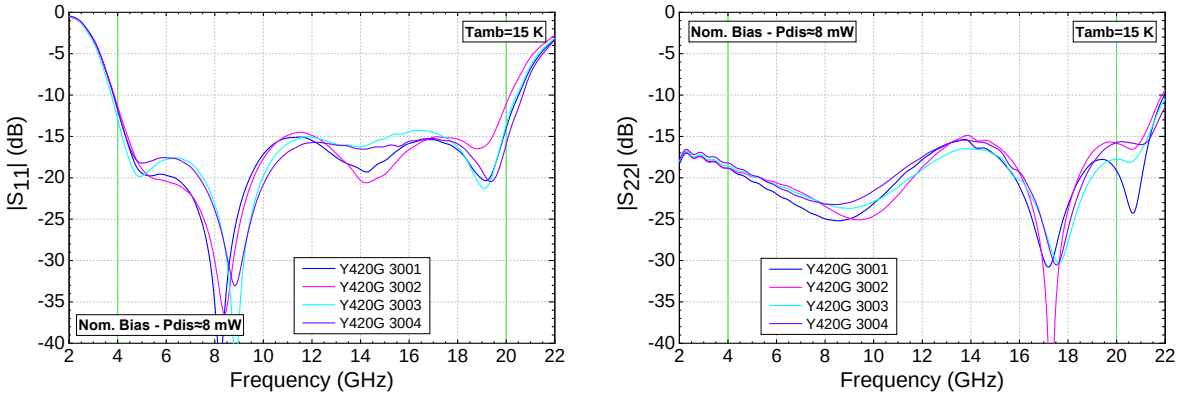

Figure 19: Comparison of the cryogenic input and output reflection of the four manufactured units of the final design. Bias settings are nominal (#1 in Table 2).

5.6 Operation for Ultra-low Power Dissipation

The power restrictions on this amplifier are a heritage of the original ALMA specifications and are motivated by the limited cooling capacity of the refrigerators. A reduction below the required 9 mW might not be strictly necessary for the actual needs (although always welcome), but could be a decisive

fact, for example, for placing the LNAs in the 4 K or 15 K stage in the cartridge of certain bands where the temperature of the mixer could be jeopardized. Moreover, it could be crucial for future developments in ALMA front-ends, like the proposed use of focal plane arrays (FPAs) which will multiply the number of receivers by the number of required pixels. This has motivated us to perform a study of the degradation in performance of an LNA with a decrease in the power consumption.

The most striking fact derived from Figure 20 is how a reduction of power to almost one third of the already low nominal bias, has such a little impact in noise temperature, of just 0.7 K. The most noticeable change in performance (see Figure 21) is the increase of the input reflection for low power at the high end of the band. On the contrary, output reflection decreases slightly.

The reduction in power produces a reduction in gain, as expected. Nevertheless, the gain levels above 30 dB even for the lowest bias are still acceptable for a cryogenic amplifier, and the gain flatness remains the same (or even improves). Another expected drawback is the deterioration of the linearity, shown in Table 5.

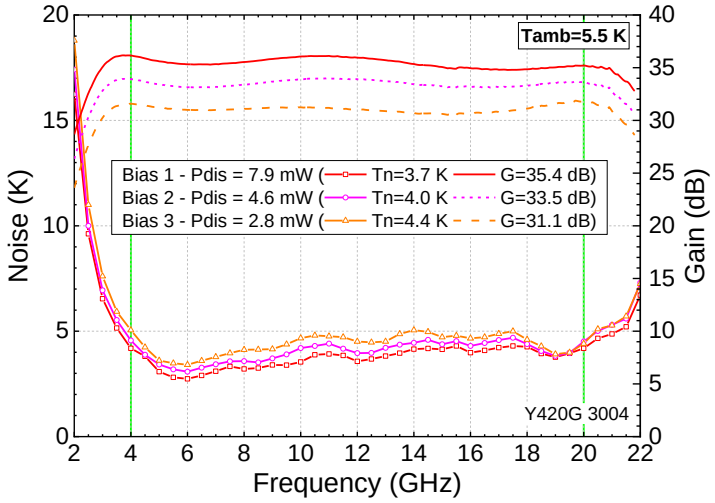

Figure 20: Comparison of the cryogenic noise temperature and gain of amplifier Y420G 3004 for different power dissipations. Bias settings are given in Table 2.

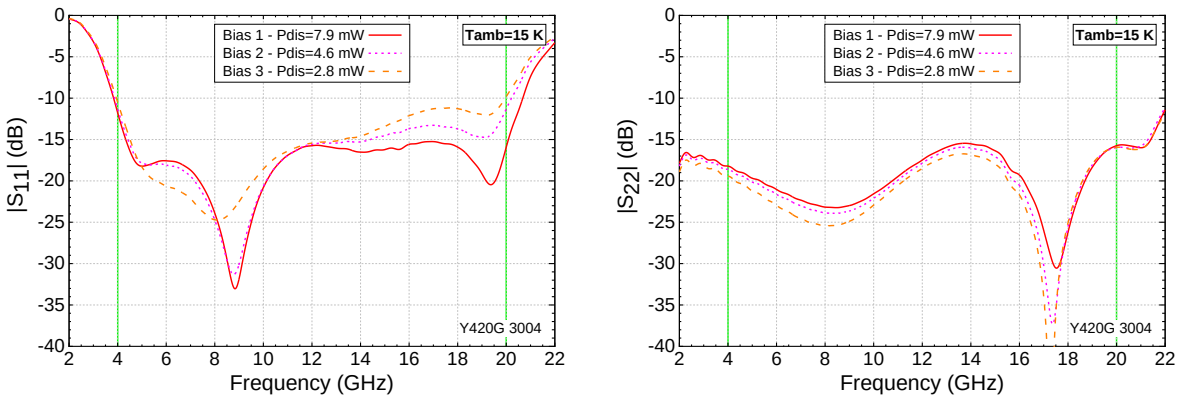

Figure 21: Comparison of the cryogenic input and output reflection of amplifier Y420G 3004 for different power dissipations. Bias settings are given in Table 2.

Table 5: Minimum 1 dB compression point of the LNA in the 4-20 GHz band for different low power bias.

Y420G 3004	Diss. power	Min. P1dB (output)
Bias #1	7.9 mW	-9.1 dBm
Bias #2	4.6 mW	-10.7 dBm
Bias #3	2.8 mW	-13.1 dBb

5.7 Balanced Amplifier Results

It is interesting to insist here in the implications of the results of the balanced amplifier presented in [15] which include two alternative design amplifiers and two specially developed 4-20 GHz 3-dB quadrature hybrid couplers. The design of the hybrids is described in Appendix 3 of [3].

As Figure 22 and Figure 23 demonstrate, a balanced architecture using these hybrids guarantees a reflection level below -20 dB with a noise penalty (at 5 K ambient) just around 1.5 K over the original single-ended amplifiers. The alternative design used has relatively good IRL, but the same improvement would apply to an amplifier design trading a noise temperature reduction for a relaxed IRL.

Furthermore, this approach, ideally, would cancel the correlated noise wave emitted by the balanced amplifier towards the input termination, suppressing the noise ripple generated by the mismatch between the mixer and the amplifier.

The possibility of halving the power dissipation with almost no consequences in noise and gain, as demonstrated in the previous section, would allow the use of such amplifiers within ALMA power specs. The only remaining drawback would be the bulk and complexity of the solution. This could be addressed by a compact design based on MMIC amplifiers and integrating the quadrature hybrids in a single module.

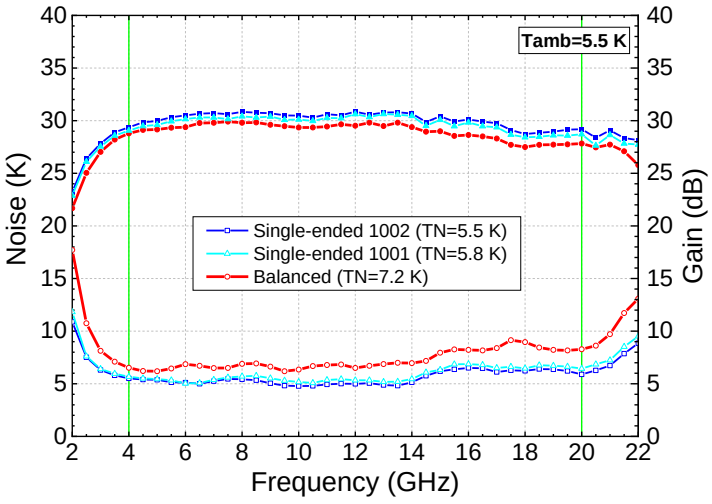

Figure 22: Noise and gain of the balanced amplifier compared with the two single-ended amplifiers of the alternative design that integrate it (Y420G 1001 and 1002). Bias settings are given in Table 2.

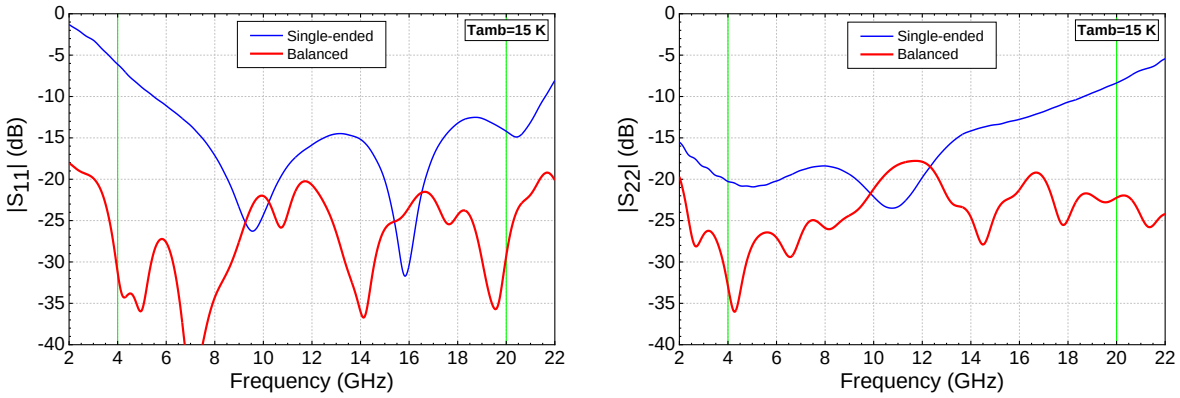

Figure 23: Input and output reflection of the balanced amplifier compared with one of the single-ended amplifiers that integrate it (Y420G 1001). Bias settings are given in Table 2.

5.8 Results in a Band 9 Receiver

As previously mentioned, two amplifiers of the alternative design (with not so good IRL in the lower part of the band and not using the optimized transistors) were sent to NOVA in order to assess the capability of their band 9 mixer to broaden the delivered IF to 16 GHz and also to test the performance of the amplifiers in a real receiver.

The amplifiers were tested with an external bias-T at the input in both a DSB and 2SB receivers equipped with band-9 type SIS mixers. The results were presented by NOVA in the final report corresponding to an ESO development study aimed to upgrade band 9 [18]. We collect here as an example one plot representing the IF power (Figure 24) and another one with the image rejection achieved (Figure 25), both for different LO frequencies across the sky band.

The first and most obvious conclusion is that the amplifiers are usable in an ALMA receiver, covering a band that extends even further down to 2 GHz. The ripple is quite low in part due to the good IRL of the amplifiers, although more elements have to be taken into consideration, like the output impedance of the mixer and the characteristics of the bias-T and the rest of the IF infrastructure.

Another conclusion is that an IF amplifier with this level of IRL allows a 2SB receiver to comply with ALMA IRR specs (10 dB) at least up to 18 GHz. The results might have been better if the data had been taken using the same IF box used for the power measurements instead of a problematic spectrum analyzer. As before, the external bias-T could also be affecting the results.

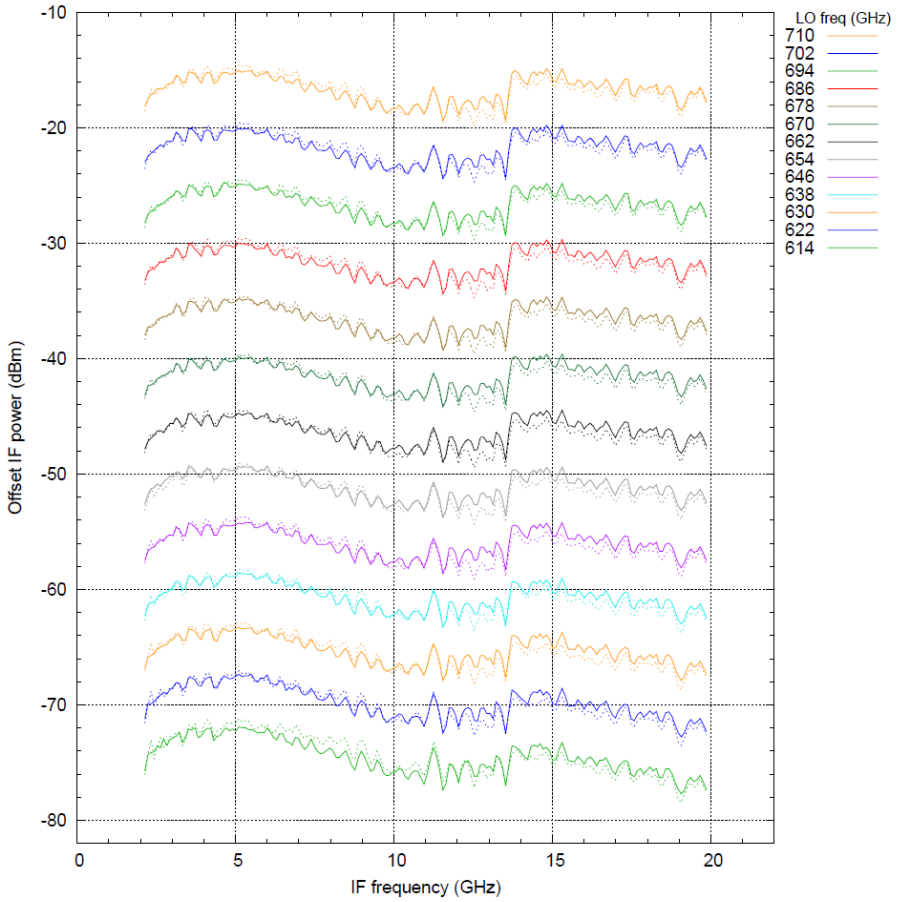

Figure 24: IF power for different LO frequencies for a 2SB mixer with IF amplifiers Y420G 1001 and 1002, looking at a 300K load. Each curve is offset vertically by a multiple of 5 dB to separate them. Solid line: USB, dotted line: LSB. Figure courtesy of NOVA, extracted from [18].

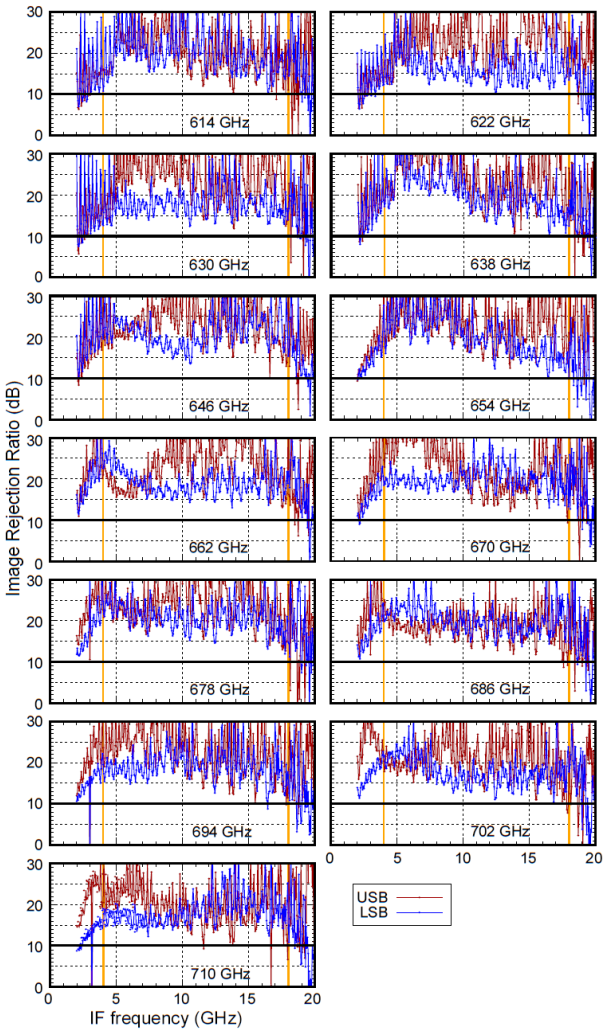

Figure 25: Image Rejection Ratio as function of IF frequency for different LO frequencies for a 2SB mixer with IF amplifiers Y420G 1001 and 1002. The thick lines at 10 dB show the typical (current) ALMA spec. Figure courtesy of NOVA, extracted from [18].

5.9 Comparison with a 2-18 GHz LNA

During the course of this project, taking advantage of the new transistor developments and of some of the findings about the use of inductors in the input matching, we decided to improve the noise performance and expand the band of our old 2-14 GHz design to 2-18 GHz. This upgrade is not as optimized as a complete redesign, but the results, presented in [28], were remarkably good.

It is worthwhile to compare this development with the 4-20 GHz amplifier, especially in the noise and input reflection results (see Figure 26). An InP HEMT amplifier with this fractional bandwidth cannot be matched in the low end of the band and no attempt was made to optimize the input reflection (hence the poor value also above 14 GHz, the original design frequency). The superiority of the present design in this aspect is evident. This poor IRL would surely affect the IRR of the 2SB receivers planned for ALMA. Some tests with this amplifier have been performed in a DSB receiver, but unfortunately, we still have no IRR measurements.

The question about how much the noise temperature could improve if the design focuses only on it disregarding the IRL cannot be answered rigorously with the data from this comparison. The 2-18 GHz is an evolution of a previous design with some constraints and a slightly better result may be possible. The average noise temperature is slightly better for the 4-20 GHz design (3.7 K vs 4.1 K).

However, the extension of the band towards lower frequencies might be appealing from a system point of view. A solution for this 2-18 GHz band could be a balanced configuration, which is feasible, as Yebes has developed 3 dB quadrature hybrid couplers for even greater fractional bandwidths (1.5-15.5 GHz). This would solve the IRR problem and at the same time, improve the noise ripple between mixer and LNA, as mentioned in section 5.7. This section also comments on some issues that would have to be addressed for this option to be applicable to an ALMA cartridge (power dissipation, bulk).

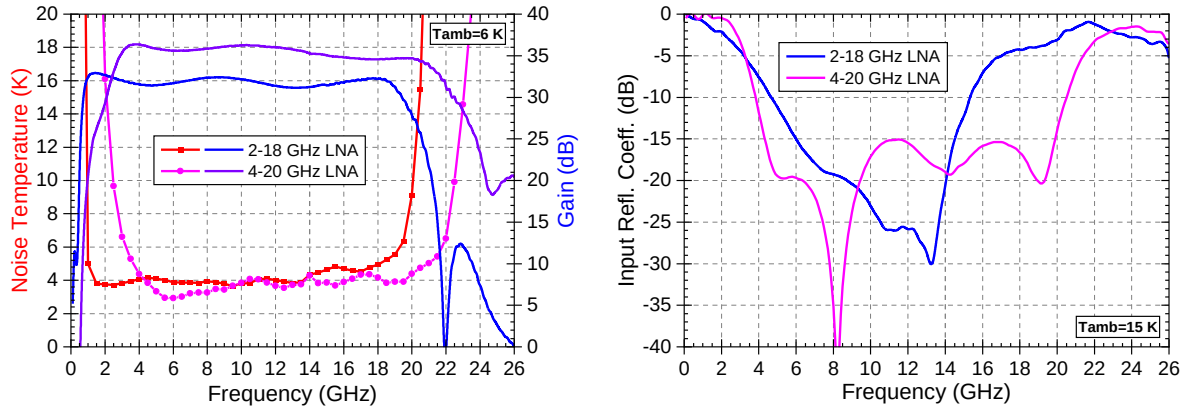

Figure 26: Comparison of the cryogenic gain and noise (left), and input reflection (right) of the final prototype amplifier Y420G 3001 with a 2-18 GHz LNA using the same transistor in the first stage. Average noise in the band is similar (4.1 K for the 2-18 GHz and 3.7 K for the 4-20 GHz). Gain is not directly comparable because the 2nd and 3rd stage devices of the 2-18 GHz are from a different foundry.

6 CONCLUSIONS, FINDINGS AND FUTURE WORKS

This report presents the summary of the work done to demonstrate an ultra-wideband, low noise, cryogenic IF amplifier fulfilling the needs of the future generation of ALMA receivers compliant with the stringent requirements of the ALMA2030 roadmap. The goal of obtaining an instantaneous bandwidth of 16 GHz with a noise temperature of 4 K and simultaneously an input reflection loss better than 15 dB seemed totally unrealistic at the start of the project. It became clear that some drastic innovations were needed to approach the target.

The InP HEMTs devices used in the amplifiers are the key for achieving the noise goal. With the help from Diramics and by drawing on additional funds from outside this project, several runs of devices with different layouts, layer structure and Schottky barrier height were developed and tested. The end result was new optimized devices with improved noise, and which also achieved the optimum at a lower bias, with the potential of reducing the power dissipation.

In addition to the HEMTs, such a demanding design required a very careful selection of passive components and very accurate models. In this context, the most remarkable innovation has been the use of new tiny thin-film resistors on quartz substrate and spiral coils with high resonance frequencies. The modeling was performed on the basis of careful probe station measurements of the components. Combining all this, a very good agreement between the models and the measurements was achieved.

Special attention was paid to the cryogenic noise characterization as well as to the other measurements of the prototypes built. This led to an upgrade of the systems used to measure noise, gain and reflection and to the realization of very accurate noise temperature measurements with the variable heated load method at different ambient temperatures.

During the development of the contract, additional results worth mentioning were obtained, such as the study of the performance of the 4-20 GHz amplifier with extremely low bias, the development of 4-20 GHz balanced amplifiers with excellent reflection and the development of other prototype amplifiers for the 2-18 GHz band.

The final prototype was an amplifier for the 4-20 GHz band with less than 4K average noise temperature (when cooled to 5 K), more than 15 dB input return loss in 95% of the band, average gain higher than 35 dB with less than 2 dB of ripple and less than 9 mW of power dissipation. Remarkably, little performance degradation was measured when reducing the power dissipation below 3 mW. The amplifier was tested for unconditional stability over a wide bias range and the repeatability and reproducibility of the design was demonstrated by comparing the results of four different units built.

This project concludes with the result of an IF amplifier that is perfectly usable for the future generation of ALMA receivers. Moreover, it has been validated by NOVA tests in a 2SB receiver featuring Band 9 SIS mixers. However, the path taken suggests possible future studies that, if successful, could introduce additional improvements. Of particular interest could be:

a) The integration of a bias T for the SIS mixer in the amplifier. Note that the realization of a bias T of such a wide band with low loss and no resonances is not a trivial task.

b) The development of an MMIC that integrates all or part of the amplifier to simplify the assembly towards an easier industrialization, applying the lessons learned in the design with discrete components.

c) The deepening in the concept of the balanced amplifier already demonstrated. This option could be a viable alternative, especially if it is possible to develop MMICs with very low power dissipation and hybrids of small size and very low losses (for example, with superconductors on quartz or silicon substrates).

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