Direct Measurement of Self-Heating Effect on Chip Resistors Used for Cryogenic Amplifiers Bias Networks

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A	2021-05-12	All	First Issue

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ABSTRACT

Modern low noise amplifiers for radio astronomy are specified with increasingly wider bandwidth, which in the case of IF amplifiers can extend from L to K band. On the one hand, this has driven the use of resistors in the bias networks with lower parasitics, which can handle very low power. On the other hand, drain currents have grown to properly bias larger transistors. To assess whether the self-heating of critical resistors can contribute significantly to the LNA noise temperature, two 50 ohm resistors in different sizes and substrates (alumina and fused quartz) have been mounted on a test fixture and used as a matched load at the input of an LNA. The power detected at the output of the LNA varying the current flow through the resistor allows a good estimation of the resistor temperature. Plots of power density versus temperature are presented. The results are in agreement with theoretical calculations. Alumina resistors hardly pose any problem in a typical amplifier despite its size, but the temperature increase in fused quartz resistors due to its low cryogenic thermal conductivity might recommend to avoid them in some cases.

1 INTRODUCTION

Cryogenic hybrid Low Noise Amplifiers use lumped chip resistors as part of the DC bias networks. Some of the resistors also perform gain stabilization or equalization functions and the thermal noise generated inside them contributes to the overall amplifier noise. In principle this noise only depends on their physical temperature. However, since in most cases some power is dissipated in them due to the bias current, the question arises whether the dissipated power can cause a significant increase in physical temperature contributing to the noise temperature of the amplifiers.

The need to increase the bandwidth of amplifiers and their central frequency has led to the search for components with lower parasitics. This has driven the use of smaller and smaller resistors and even to change their support material from alumina to fused quartz (with lower dielectric constant). Both contribute to increase the thermal resistance and thus aggravate the self-heating problem.

Moreover, these ultra-wide bands start at relatively low frequencies, requiring wide gate transistors in the amplifiers in order to achieve an acceptable noise and power matching. The optimal bias current driving these devices scales with the gate size, so the power dissipated in the drain resistors of the bias networks is comparatively higher. Figure 1 illustrates the estimated impact in noise performance on a wide band amplifier due to an increase of 50 K in the temperature of the 100 ohm drain resistor.

This work reports the results obtained from the measurement of the noise generated in two very small size chip resistors, of alumina and fused quartz, cooled to cryogenic temperature, as a function of the power dissipated.

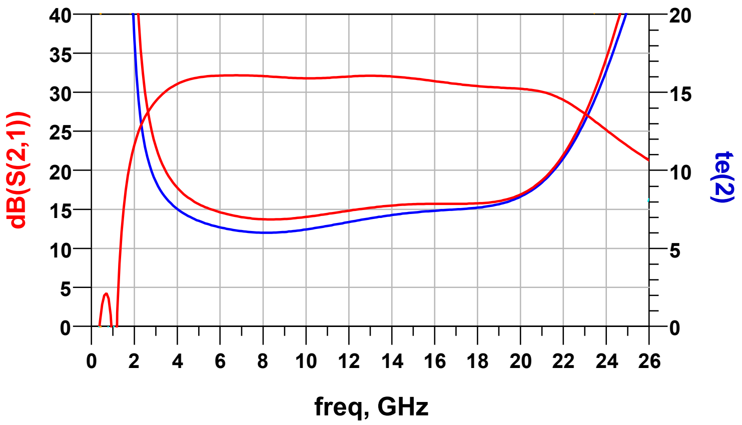


Figure 1: Noise increase in an ultra-wide-band (4-20 GHz) amplifier (Y420G1) assuming that the 100 ohm drain resistor is 50 K hotter than the ambient 12 K temperature.

2 TEST FIXTURE, LNA AND TEST EQUIPMENT

To perform the measurements, a small box was used to house a 50 Ohm microstrip line, a conical coil for polarization, a decoupling capacitor and the 50 Ohm chip resistor to be characterized[1]. Accurate noise measurements require a good match of the input termination. With this type of construction this is achieved in a limited frequency range.

Figure 2 and Figure 3 show the test fixture with the 50 ohm resistors used (datasheets in Appendix I):

- Compex MN1-20-20X10X10-A-50R00-J-VB: **Quartz** resistor, 20×10×10 mil.
- State of the Art S 0202 AA 500 JKW: **Alumina** resistor, 20×20×10 mil.

Figure 4 shows the input reflection of the test fixtures measured at room temperature. The best results are obtained around 700-1000 MHz. It was decided to perform the measurements at 700 MHz.

Note that to achieve better matching, short bond wires were used at both resistor pads. This might not be representative of a standard arrangement of an LNA drain resistor, which typically uses longer wires connected to lines or chips and not directly to the base plate, leading to a less efficient heat power drain.

The resistors were glued to the gold-plated aluminum base with conductive epoxy Epotek H-20. Thermal conductivity of this epoxy at cryogenic temperature is low [2]; the thickness of the layer of epoxy must be considered when estimating the thermal resistance of the path to the base plate. In the particular arrangement of this setup[2] the thickness of the epoxy layer is around 25 µm instead of the usual 10 µm.

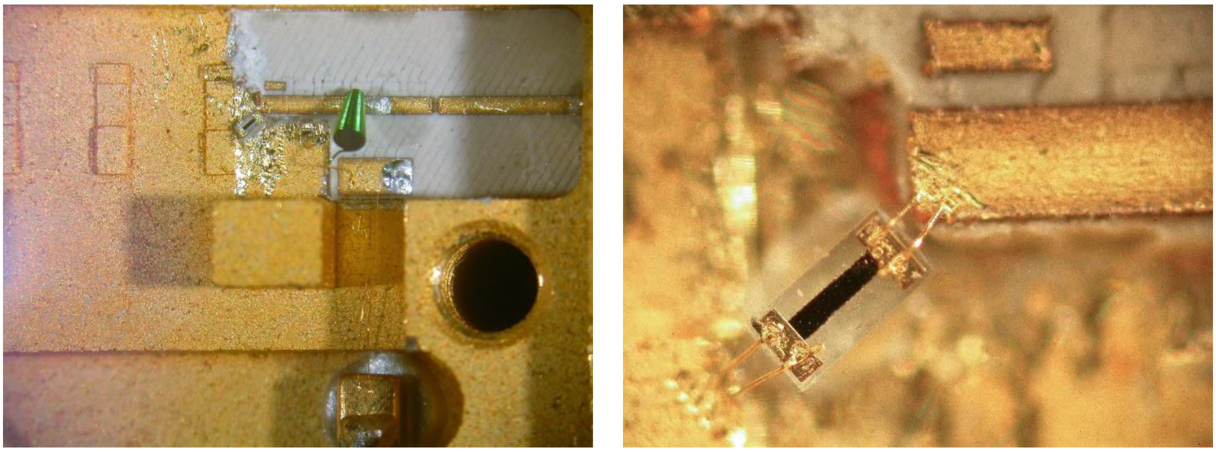


Figure 2: Compex quartz resistor test fixture (left) and detail of the resistor bondings (right).

[1] The box and 50 ohm lines used were originally produced for wide band LNAs (series Y214G).

[2] The resistors were mounted partly on top of the base metallization of the substrate, which was exposed because it had to be manually cut to adapt it to this particular setup.

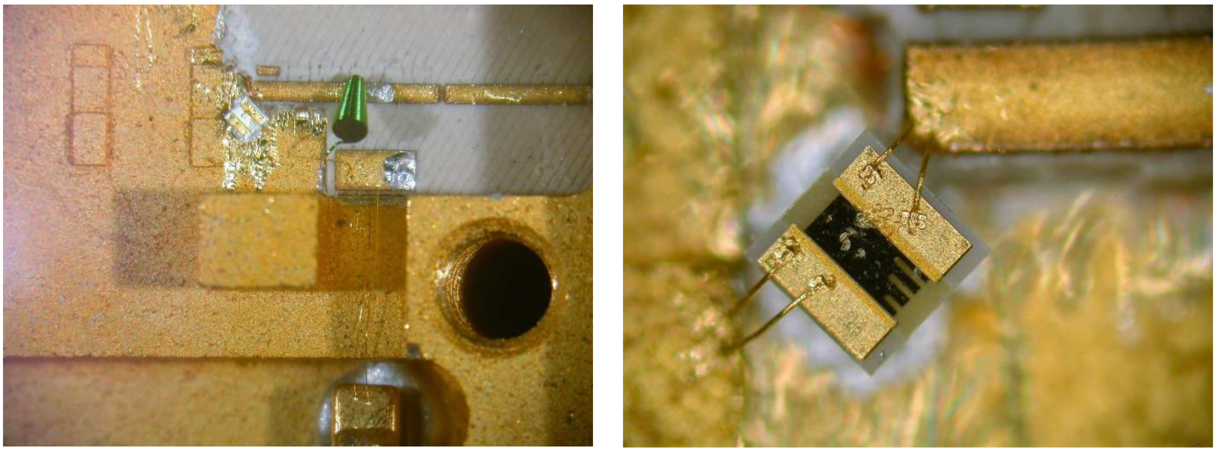


Figure 3: SOTA alumina resistor test fixture (left) and detail of the resistor bondings (right).

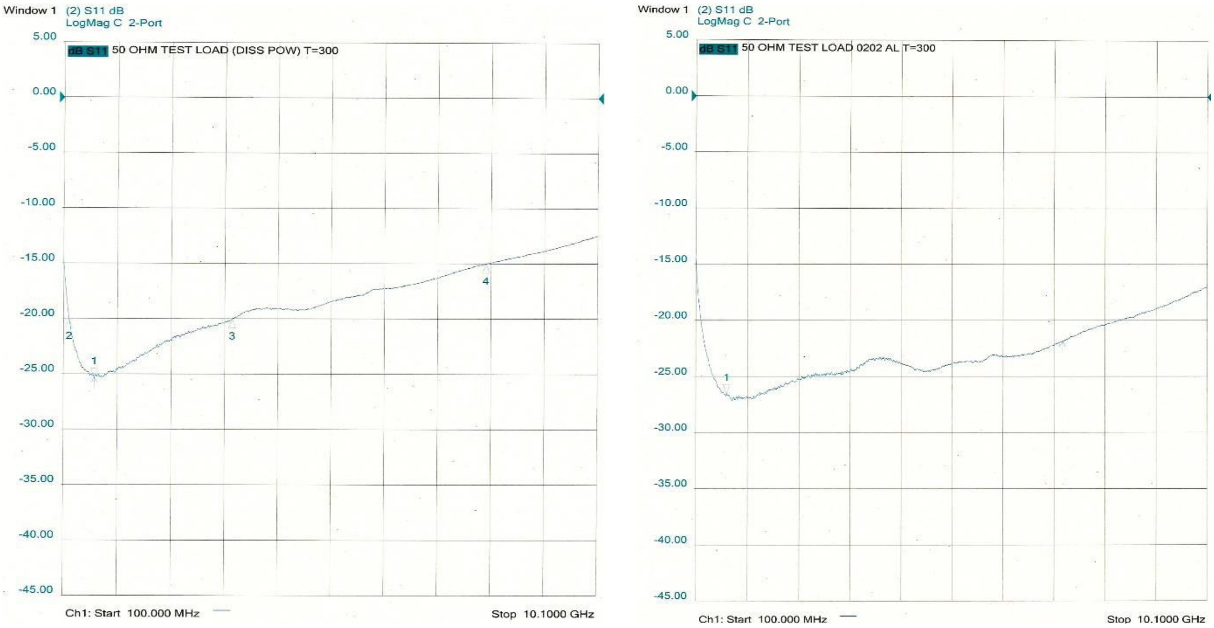


Figure 4: Room temperature input reflection of the two 50 ohm resistors tested, mounted in the module. On the left, the quartz chip from Compex, size 0102. On the right, the alumina chip from SOTA, size 0202. Markers are placed at 700 MHz.

The accurate measurement of the low noise generated in the input termination requires a low noise cryogenic amplifier with good gain stability and low input reflection in this frequency range. It was decided to use a SiGe unit (YSG 2001) which was available at the time of the measurement with good performance at low frequency.

The noise measurements were performed with a PNA-X N5247A Vector network analyzer [3] (10 MHz-67 GHz) with option 029 (Source-Corrected Noise Figure Measurements) (Keysight). The receiver noise temperature was measured with a noise source HP 346C.

3 MEASUREMENTS

The measurements were obtained by cooling the amplifier to either 7 K or 15 K. The temperature was stabilized by a PID loop with the sensor attached to the amplifier. The test fixture with the resistor was directly connected to the input of the amplifier although different thermal straps were used for connecting each component to the refrigerator cold plate. The final temperature of the resistor module was colder than the amplifier: 5.5 K and 13.9 K respectively. A photograph of the measurement setup is shown on Figure 5.

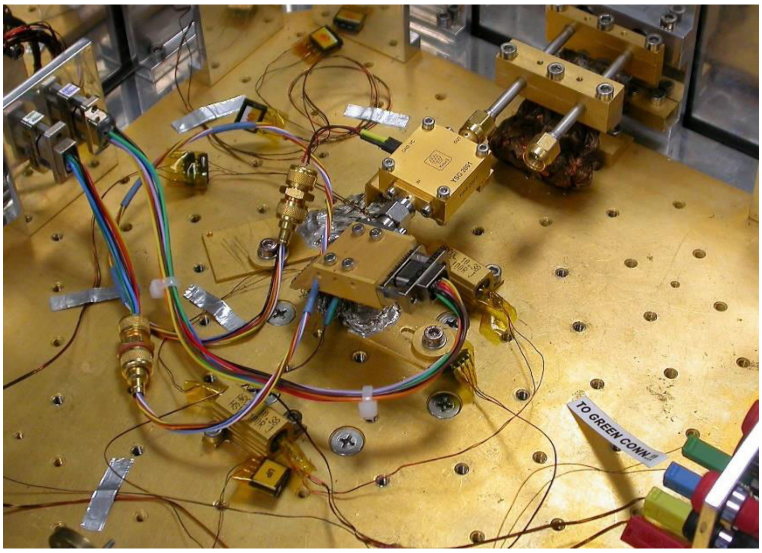


Figure 5: Module with the load connected to the LNA for cryogenic measurements in the SUMI-1 cryostat.

The noise temperature and gain of the cryogenic amplifier was accurately known by previous measurements at the working temperatures obtained by the heated load method. The goal is to determine the temperature of the input termination (chip resistor tested) by the excess noise measured when bias is applied. The temperature of the "hot" resistor can be calculated as:

$$T_h = \left(T_c + T_{sys}\right)\frac{P_h}{P_c} - T_{sys}$$

Where:

- P_h is the total output noise power measured (in linear units) with bias applied.
- P_c is the total output noise power measured (in linear units) without bias applied.
- T_c is the physical temperature of the resistor with no bias (measured by a sensor in the fixture).
- T_{sys} is the noise temperature of the amplifier and the receiver cascaded.

The system noise temperature can be obtained as:

$$T_{sys} = T_{LNA} + \frac{T_{RX}}{G_{LNA}}$$

Where:

- T_{LNA} is the noise temperature of the amplifier.
- T_{RX} is the noise temperature of the receiver (PNA-X).
- G_{LNA} is the gain of the amplifier (in linear units).

Note that the measurement obtained depends on the relation between the values of total output noise powers as in Y-factor measurements.

4 Results

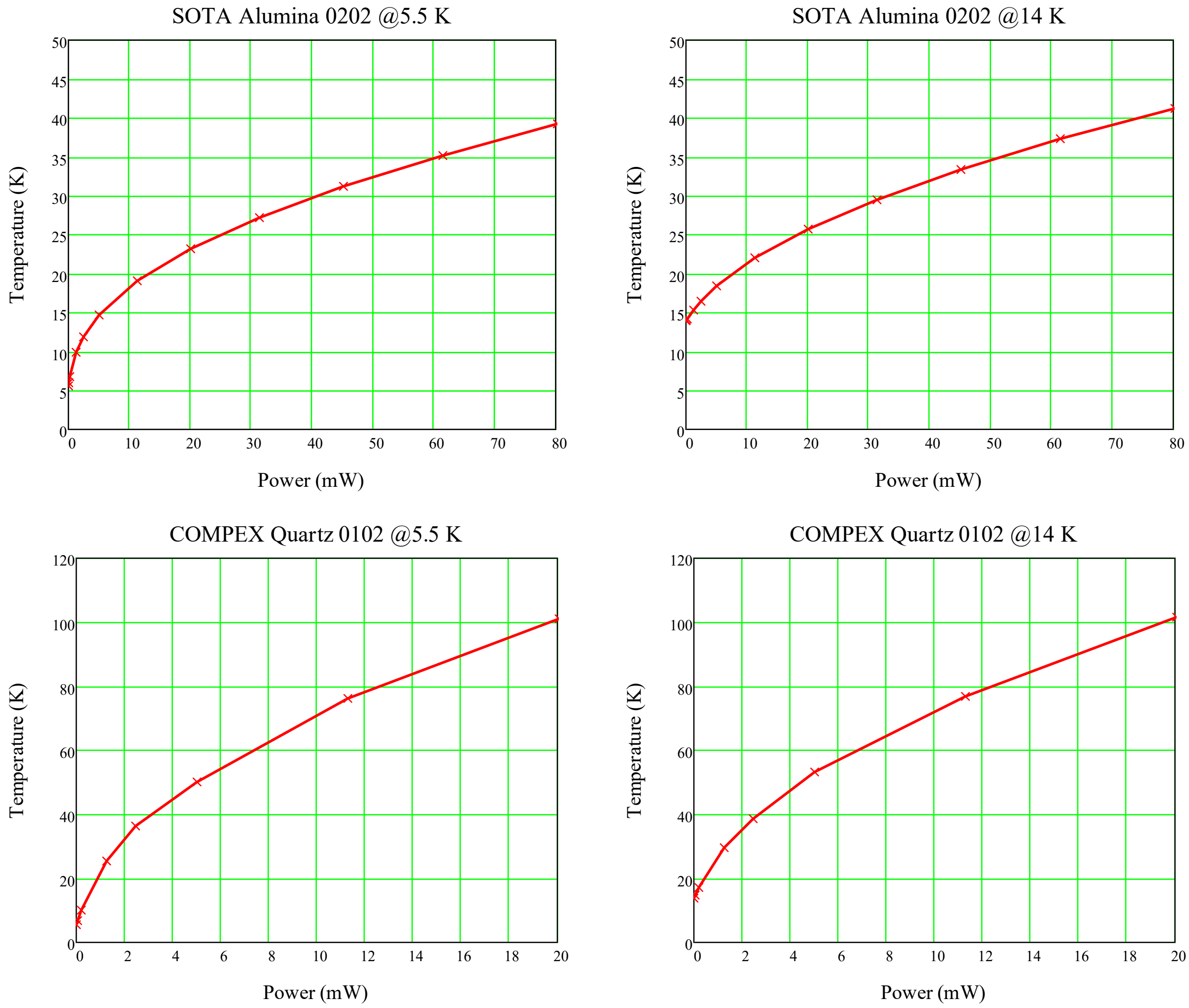


Figure 6: Measured temperature of the 50 ohm resistor as a function of the dissipated power. On the top row, SOTA Alumina resistor, size 0202 and on the bottom row, COMPEX Quartz resistor, size 0102. On the left, fixing the LNA temperature to 7 K (unbiased resistor @5.5 K). On the right, fixing the LNA temperature to 15 K (unbiased resistor @13.9 K).

Compex 0102 Quartz resistor

Power (mW)	T_h (K)	T_h (K)
0	5.482	13.79
0.05	6.754	14.693
0.2	10.029	17.104
1.25	25.374	29.587
2.45	36.286	38.593
5	50.097	53.186
11.25	76.166	76.805
20	101.045	101.532

SOTA 0202 Alumina resistor

Power (mW)	T_h (K)	T_h (K)
0	5.59	13.95
0.05	5.967	14.044
0.2	6.757	14.186
1.25	9.89	15.306
2.45	11.859	16.434
5	14.68	18.409
11.25	19.073	22.02
20	23.173	25.71
31.25	27.175	29.464
45	31.211	33.38
61.25	35.169	37.32
80	39.236	41.209

5 THEORETICAL ESTIMATION OF THE TEMPERATURE RISE

Knowing the thermal conductivity $k(T)$ we can estimate the temperature rise in the resistor due to the power dissipated according to the Fourier law for the heat flux $\overrightarrow{\Phi_q}$:

$$\overrightarrow{\Phi_q} = -k(T) \cdot \nabla T$$

Assuming a uniform heat distribution and a unidimensional heat flux, and neglecting the radiated power, the previous expression in integral form is:

$$P = \frac{S}{h} \cdot \int_{T_1}^{T_2} k(T)\, dT$$

Where:

- P is the power transmitted from 2 to 1 (in our case, the top and bottom of the resistor)
- T_1 and T_2 are the temperatures of 1 and 2 respectively (top and bottom of the resistor)
- S is the surface across which the power is transmitted (the resistor surface)
- h is the distance between 1 and 2 normal to S (height of the resistor and epoxy)
- $k(T)$ is the thermal conductivity of the path (resistor and epoxy)

The last equation is thus solved for T_2 assuming that P is the power dissipated in the resistor.

Cryogenic data for alumina and quartz thermal conductivity can be obtained from [1], see Figure 7.

The contribution of the thermal resistance of the epoxy has been taken into account, as it is significant especially in the case of the alumina resistor, with higher thermal conductivity. Cryogenic data for Epotek H-20 thermal conductivity was obtained from [2], see Figure 8.

The power drain through the bond wires has been neglected.

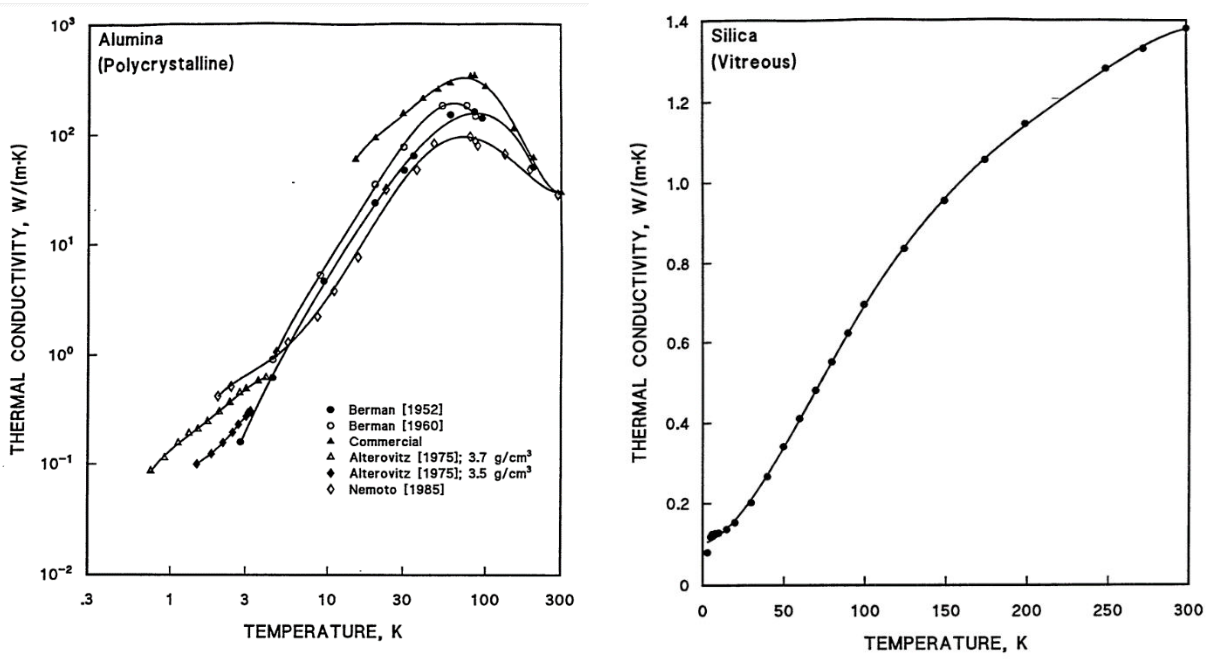


Figure 7: Thermal conductivity of alumina and fused quartz. For alumina we use the data from Nemoto (1985). The curve for fused quartz is from Touloukian (1970).

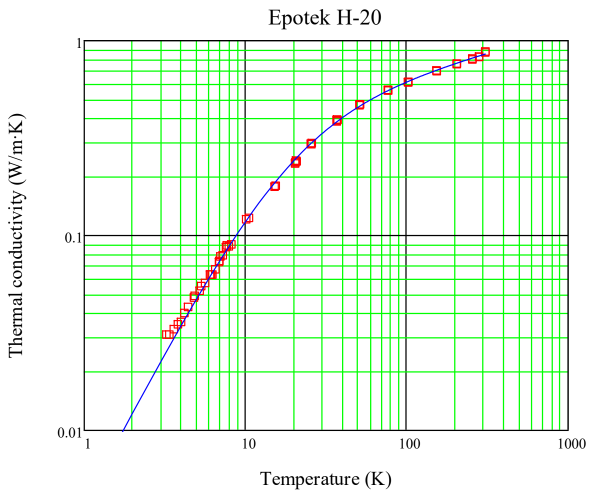


Figure 8: Thermal conductivity of Epotek H-20 epoxy according to Amils (2017).

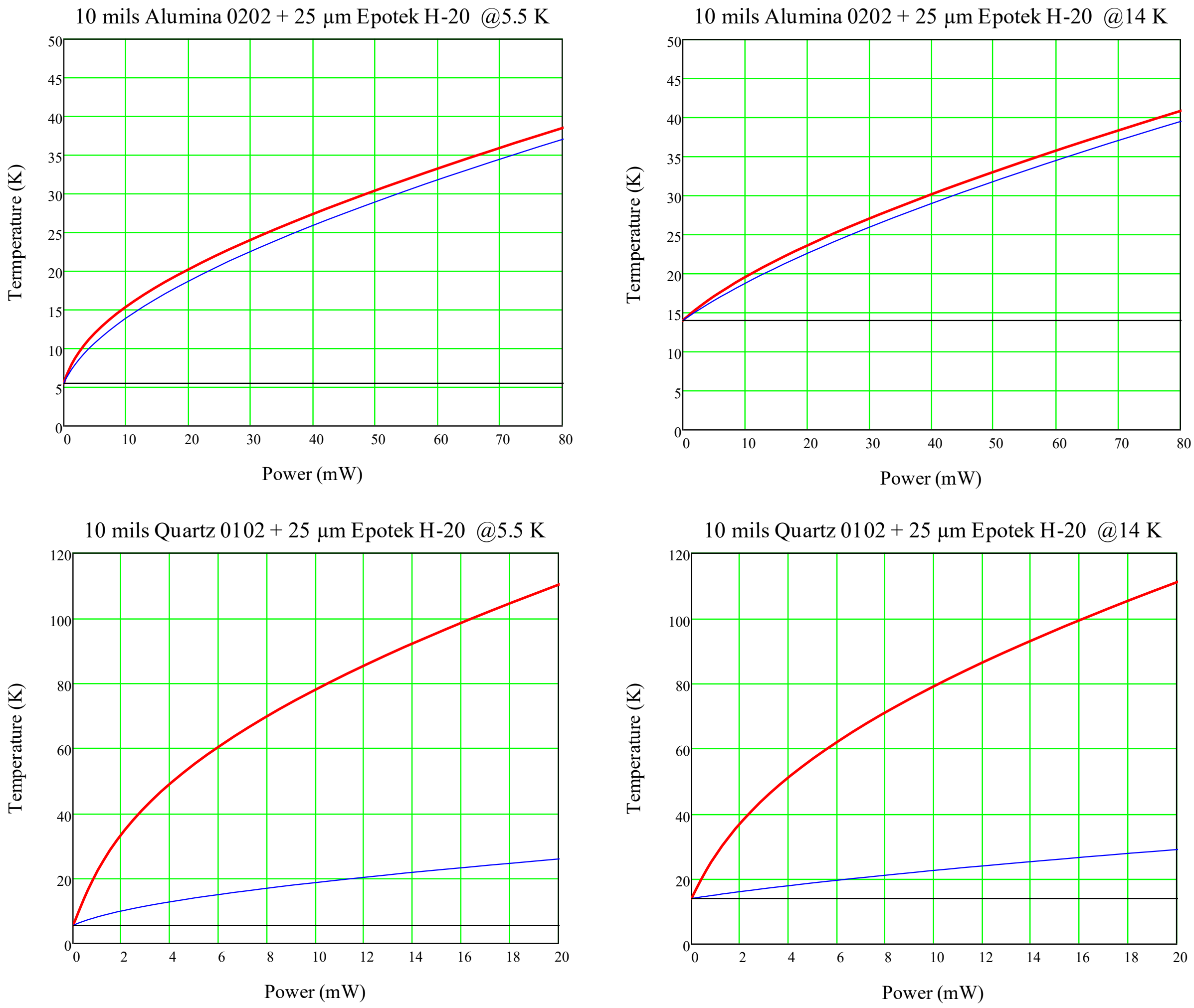


*Figure 9: Estimated temperature of the resistor as a function of the dissipated power. Curves for quartz and alumina at 5.5 K and 14 K using the **estimated epoxy thickness** of the samples (25 µm). In red, the temperature of the resistor thin film. In blue, the temperature of the base of the resistor (top of the epoxy). In black, the temperature of the base plate.*

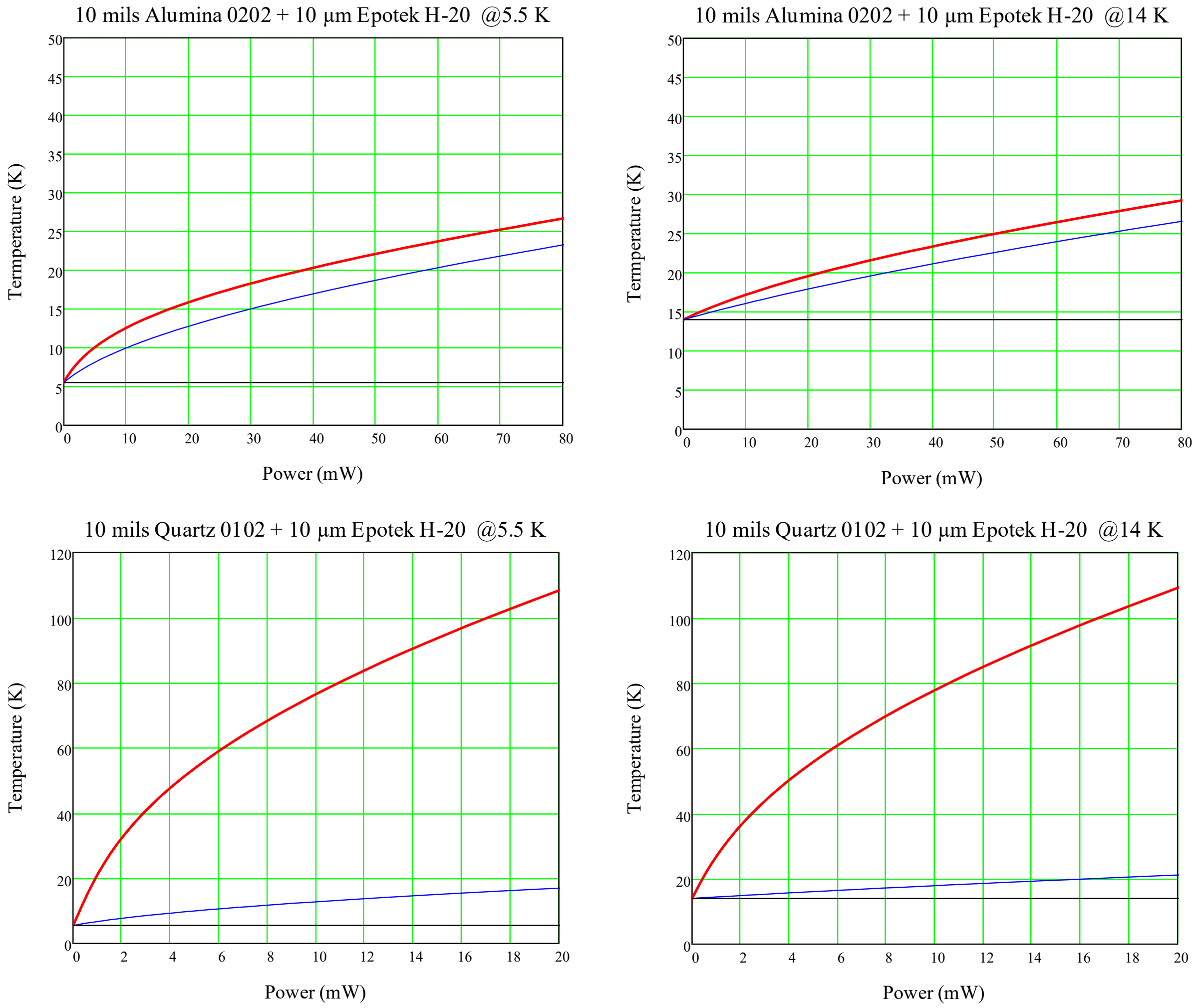


Figure 10: Estimated temperature of the resistor as a function of the dissipated power. Curves for quartz and alumina at 5.5 K and 14 K using the ***typical epoxy thickness*** *(10 µm). In red, the temperature of the resistor thin film. In blue, the temperature of the base of the resistor (top of the epoxy). In black, the temperature of the base plate.*

6 Scaling the Results

The results can be scaled with the surface of the resistor to extrapolate to other sizes.

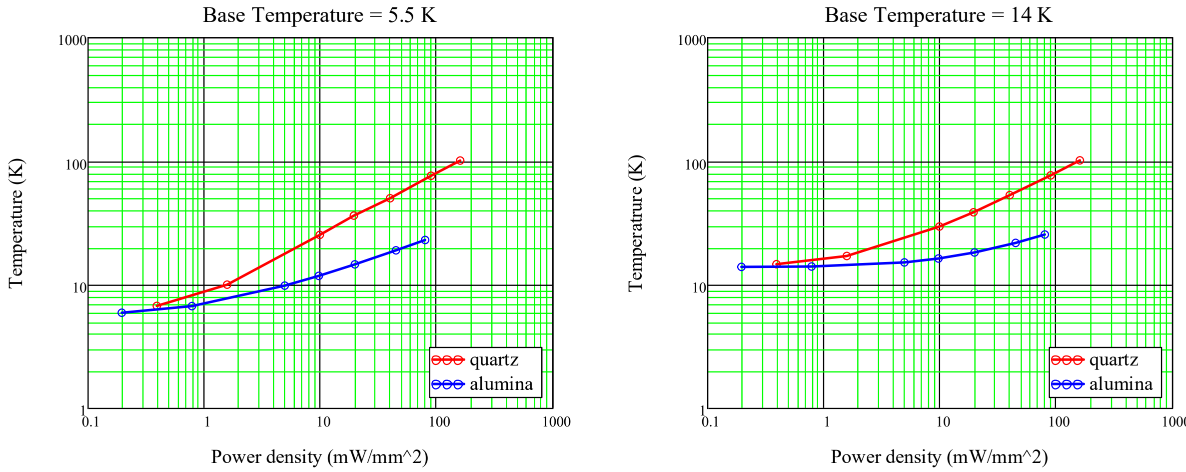


Figure 11: Measured temperature of the alumina (blue) and quartz (red) resistor as a function of the dissipated power density. On the left for a base temperature of 5.5 K. On the right for 13.9 K.

Remember that the epoxy thickness in this test fixture was around 25 µm. The estimations for a standard thickness of epoxy of 10 µm are shown in the following plots (no bond wires included).

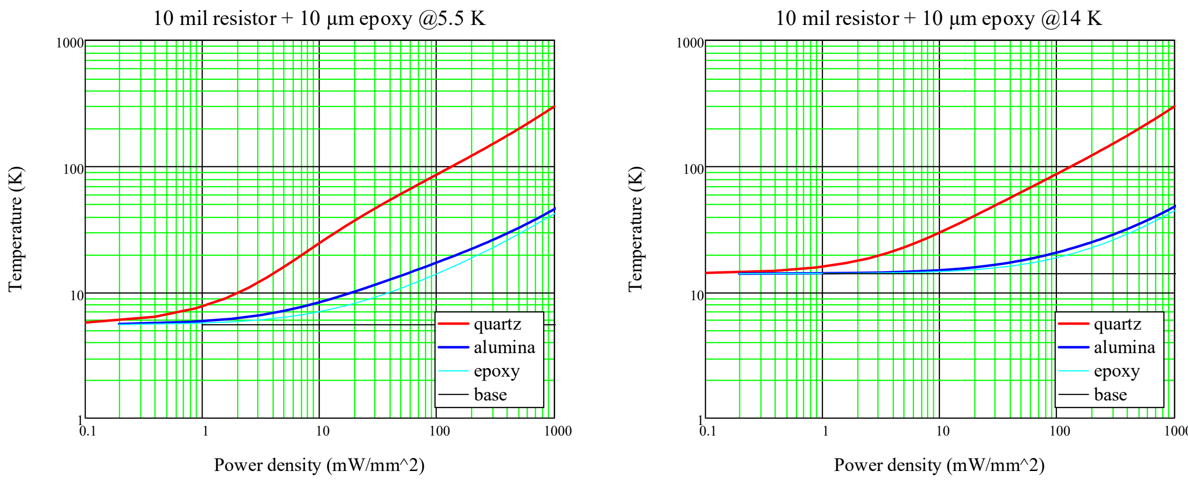


Figure 12: Estimated temperature of a 10 mil thick block of alumina (blue) and quartz (red) glued with 10 µm of Epotek H-20, as a function of the dissipated power density. On the left for a base temperature of 5.5 K. On the right for 13.9 K.

7 CONCLUSIONS

The power dissipation in the resistors usually employed in cryogenic low noise amplifiers is responsible for a temperature increment that is only significant in terms of noise temperature variation under very specific circumstances. The resistors must be small in size, high in value and support a high current (high power density), but even then, only with low thermal conductivity substrates the heating is important. Alumina resistors can withstand power densities of 80 mW/mm^2 at 14 K with a temperature rise of less than 6 K (that is about 10 mA on a 100 ohm 0102 resistor). On the contrary, the use of fused quartz resistors must be carefully evaluated.

The agreement between the measurements and the simulations is quite good (compare Figure 6 and Figure 9), allowing us to estimate a correction for the excess of epoxy in the samples (as compared with a typical assembly). This was the cause of the extra dissipation noted specially in the alumina resistor. Figure 12 can be used to calculate the temperature rise in the resistor for any given power density.

REFERENCES

[1] N. J. Simon, "Cryogenic properties of inorganic insulation materials for ITER magnets; A review," National Institute of Standards and Technology, Boulder, NISTIR 5030, Dec. 1994; available at https://nvlpubs.nist.gov/nistpubs/Legacy/IR/nistir5030.pdf

[2] Ricardo I. Amils, "Amplificadores criogénicos de bajo ruido para aplicaciones radioastronómicas y espaciales," PhD Thesis Dissertation, Madrid, 2017, available at https://eprints.ucm.es/id/eprint/47612/

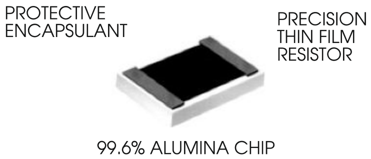
[3] J.D. Gallego, R. Amils, C. Diez González, I. López, I. Malo "Using Keysight PNA-X and NFA Noise Receivers for Noise Temperature Measurements with Cryogenic Variable Temperature Loads," CDT Technical Report 2019-17, available at https://icts-yebes.oan.es/reports/doc/IT-CDT-2019-17.pdf

APPENDIX I: DATASHEETS

State of the Art, Inc.

0202 Thin Film Chip Resistor

Standard Grade, Surface Mount, Solderable



FEATURES

- Tolerances to ± 0.1%
- Operating temperature range : -55° C to +150° C
- For high-density hybrid circuits where space is at a premium
- TCR's to ± 25 ppm
- Made with the same materials and process as our MIL-PRF-55342 "S" level qualified chips
- Delivers greater power handling capability with lighter weight construction

PERFORMANCE CHARACTERISTICS

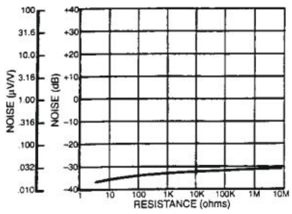
Resistance Range	5Ω – 35KΩ
Tolerances	0.1%, 0.25%, 0.5%, 1%, 2%, 5%, 10%
Maximum Power	25 mW
Maximum Voltage	20 Volts

ENVIRONMENTAL PERFORMANCE (1)

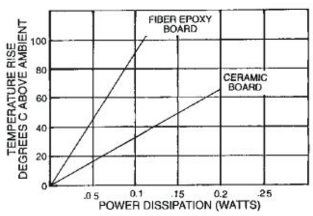
TCR (-55 to +125 °C in ppm/°C)	< 25 ppm
Thermal Shock	±0.02%
Low Temperature Operation	±0.02%
Short-time Overload	±0.02%
Resistance to Bonding Exposure	±0.02%
Moisture Resistance	±0.03%
High Temperature Exposure	±0.03%
Life	See Chart

(1) Typical resistance change, the maximum is the same as MIL-PRF-55342. Test methods are per MIL-PRF-55342.

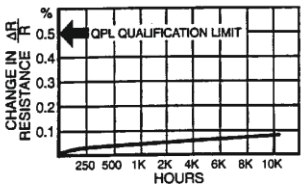
CURRENT NOISE



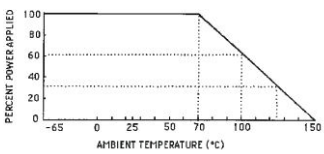
POWER DISSIPATION



TYPICAL LIFE TEST PERFORMANCE



POWER DERATING



PART NUMBERING

S0202AA 150 J H W

- Termination Material
  W: Gold
- TCR
  E: ±25 ppm H: ±50 ppm K: ±100 ppm
- TOLERANCES
  B: 0.1% C: 0.25% D: 0.5% F: 1% G: 2% J: 5% K: 10% M: 20%
- RESISTANCE VALUE
  Three or four digits are used with all leading digits significant. Four digits are used for 1% tolerance or lower, otherwise three digits are used. The last digit specifies the number of zeros to add. The letter "R" is used to represent the decimal for fractional ohmic values. Example: 5R6 is 5.6 ohms.
- Substrate Matieral A: Alumina Ceramic
- Termination Style A: Top Sided with Bottom Isolated

MECHANICAL

	INCHES	MM
Length	.020 (+.002/-.002)	.51 (+.05/-.05)
Width	.020 (+.002/-.002)	.51 (+.05/-.05)
Thickness	.009 - .011	.23 - .27
Top Term.	.004 - .006	.10 - .15

Approx. Weight .00043 grams

All product is tested IAW Mil-Std-202, method 208, including 8 hour steam aging.

PACKAGING

Two packaging options are available:

- Bulk Packaging - (5000 per Bag Max.)
- Waffle Pack - (400 per Tray Max.)

OPTIONS

SOTA offers a full line of component parts in the 0202 size including High-Reliability (customer specified testing). Available options are epoxy bondable and wire bondable terminations, and custom part marking.

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Phone (814) 355-8004 Fax (814) 355-2714 **Toll Free 1-800-458-3401**

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R Series

Thin Film Resistors – Top Side Terminations

Compex's line of wire-bondable thin film resistors offers our customers significant flexibility to meet the most challenging designs. Built to the customer's exact specifications, available alternatives include single, dual, center-tap, array, and custom configurations. Standard and microwave frequency options up to 40 GHz or higher are available, voltage rating up to 100V.

- CUSTOM MANUFACTURED TO PROVIDE THE OPTIMUM PART FOR EACH APPLICATION
- ALUMINA, ALUMINUM NITRIDE, BERYLLIUM OXIDE, SILICON, AND QUARTZ
- TOLERANCE DOWN TO 0.01%

R Part Number Assembly

Example shown: Compex Series R, center tap TaN resistor, C-35 (alumina), .020" x .020" x .010", PdAu bonding pad, bottom side bare, 1000Ω ± 5%, 150 PPM TCR, regular trim 100 mW

R T 2 - 35 - 20 x 20 x 10 – A – 10000 – J – Q E

Resistor Style
M (Microwave)
R (Standard – DC to 500 MHz)

Resistive Metallization
T (Tantalum Nitride) or
N (NiChrome)

Number of Resistors per Device

Material Type
See R Selection Charts (at right)

Length x Width (mils)
See R Chip Dimensions (at right)

Thickness (mils)
10 mil standard (exception 12 x 9 size, standard is 5 mils).
Other thicknesses available, please consult factory.

Bonding Pad Metallization
See R Selection Charts (at right)

Power Handling Code
from Table (at right)

Temperature Coefficient
of Resistance (TCR)
See R Selection Charts (at right)

Resistance Tolerance
See R Resistance Tolerance
Codes (below)

Resistance (Ω)
First 4 digits represent significant figures and the last, the number of zeros to follow. When required, the "R" is used as a decimal point and the succeeding digit represents significant figures only.e.g.: 10001 = 10000 Ω, 10000 = 1000 Ω, 100R5 = 100.5 Ω

Note: Standard dimensional tolerance for length and width is ± 2 mils. The thickness tolerance is ± 1 mil.

Standard Resistance Tolerance Codes

Tolerance	Code	Tolerance	Code	Tolerance	Code	Tolerance	Code
± 20%	**M**	± 5%	**J**	± 1%	**F**	±.05%	**Q**
± 15%	**L**	± 3%	**H**	± .5%	**D**	±.01%	**S**
± 10%	**K**	± 2%	**G**	±.1%	**B**		

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R Selection Charts

Note: Selection Charts are for guidance only. All Compex parts are built to specific customer requirements.

Microwave Resistance Range by Case Size (Ohms)

Case Size Mils	Min	Max
12X9	4	500
14X12	4	750
20X10	6	1000
15X15	4	1000
20X20	4	1250
30X20	4	2500
40X20	4	3750
30X30	2	2500
35X35	2	3000
40X40	2	3750
50X25	3	5000
60X30	3	5000
50X50	2	5000
60X60	2	5000
80X50	2	5000
100X50	2	5000
120X60	2	5000
100X100	2	5000

Standard Resistance Range by Case Size (Ohms)

Case Size Mils	Min*	Max Alumina	Max Silicon
12X9	1-3	25K	150K
14X12	1-3	40K	200K
20X10	1-3	60K	250K
15X15	1-2	70K	500K
20X20	1-2	125K	750K
30X20	1-2	200K	1M
40X20	1-2	250K	1.5M
30X30	1-2	275K	2M
35X35	1-2	300K	3M
40X40	1-2	500K	5M
50X25	1-2	300K	3M
60X30	1-2	500K	6M
50X50	1-2	700K	7M
60X60	1-2	2M	15M
80X50	1-2	2M	20M
100X50	1-2	2.5M	25M
120X60	1-2	3M	30M
100X100	1-2	3.5M	35M

Minimum Power Handling by Material and Size**

Case Size Mils	Alumina C-35	Silicon C-22	AlN C-28	BeO C-25	Quartz C-20
12X9	50 mW	50 mW	200 mW	400 mW	10 mW
14X12	100 mW	100 mW	400 mW	800 mW	20 mW
20X10	100 mW	100 mW	400 mW	800 mW	20 mW
15X15	100 mW	100 mW	400 mW	800 mW	20 mW
20X20	250 mW	250 mW	1.0 W	2.0 W	50 mW
30X20	250 mW	250 mW	1.0 W	2.0 W	50 mW
40X20	250 mW	250 mW	1.0 W	2.0 W	50 mW
30X30	250 mW	250 mW	1.0 W	2.0 W	50 mW
35X35	250 mW	250 mW	1.0 W	2.0 W	50 mW
40X40	350 mW	350 mW	1.4 W	2.8 W	70 mW
50X25	350 mW	350 mW	1.4 W	2.8 W	70 mW
60X30	500 mW	500 mW	2.0 W	4.0 W	100 mW
50X50	500 mW	500 mW	2.0 W	4.0 W	100 mW
60X60	500 mW	500 mW	2.0 W	4.0 W	100 mW
80X50	500 mW	500 mW	2.0 W	4.0 W	100 mW
100X50	500 mW	500 mW	2.0 W	4.0 W	100 mW
120X60	750 mW	750 mW	3.0 W	6.0 W	125 mW
100X100	750 mW	750 mW	3.0 W	6.0 W	125 mW

Power Handling Codes

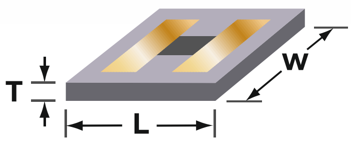
Watts	Code
10 mW	A
20 mW	B
50 mW	C
75 mW	D
100 mW	E
150 mW	F
250 mW	G
500 mW	H
750 mW	J
1 W	K
2 W	L
3 W	N
4 W	P
5 W	Q
10 W	S
15 W	T
20 W	V
25 W	W
50 W	X

*Min Value TCR 150 ppm for TaN and 25 ppm for NiC.
**Higher Power ratings available, please consult factory.

Bonding Pad Metallizations		
Metallization		**Code**
Pd/Au Top Side	Bare Bottom Side	A
Pd/Au Top Side	Ta/Pd/Au Bottom Side	D
Pd/Au Top Side	Ti/Pt/Au Bottom Side	L
Ni/Au	Application Specific	P
TiW/Au Top Side	Bare Bottom Side	E
TiW/Au Top Side	Ta/Pd/Au Bottom Side	F
Window	Silicon Only	W
Custom	Application Specific	X

Temperature Coefficient of Resistance	
Parts Per Million (PPM)	**Code**
±150	Q
±100	V
±50	W
±25	X
±10	Y
±5	Z

R Chip Dimensions



Testing Performed	Specification/Standard
Visual Inspection	MIL-PRF-55342 Para 4.8.1 MIL-STD-883 Method 2032
Mechanical Inspection	MIL-PRF-55342 Para 4.8.1
DC Resistance	MIL-PRF-55342 Para 4.8.2 MIL-STD-202 Method 303
Resistance Temperature Characteristic (TCR)	MIL-PRF-55342 Para 3.16 MIL-STD-202 Method 304
Short Time Overload	MIL-PRF-55342 Para 3.12
High Temperature Exposure	MIL-PRF-55342 Para 3.13
Thermal Shock	MIL-PRF-55342 Para 3.9 MIL-STD-202 Method 107
Resistance to Bonding Exposure	MIL-PRF-55342 Para 3.14.2
Wire Bonding Integrity	MIL-PRF-55342 Para 4.8.13
Life Test	MIL-PRF-55342 Para 3.17 MIL-STD-202 Method 108 (rated voltage @ 70°C for 2000 hours)

Performance Specifications

Typical Compex commercial testing includes 100% visual, mechanical, resistance, short time overload, and Resistance Temperature Characteristic. Our parts also meet or exceed additional MIL-PRF-55342 and MIL-STD-202 requirements outlined in the table at left. Please consult the factory for your exact testing requirements.

Higher power ratings, additional sizes, and custom resistors available. Please contact factory to request free samples.

Compex 17

APPENDIX II: EXAMPLES OF MATHCAD FILES USED

Temperature increase of cryogenic resistor

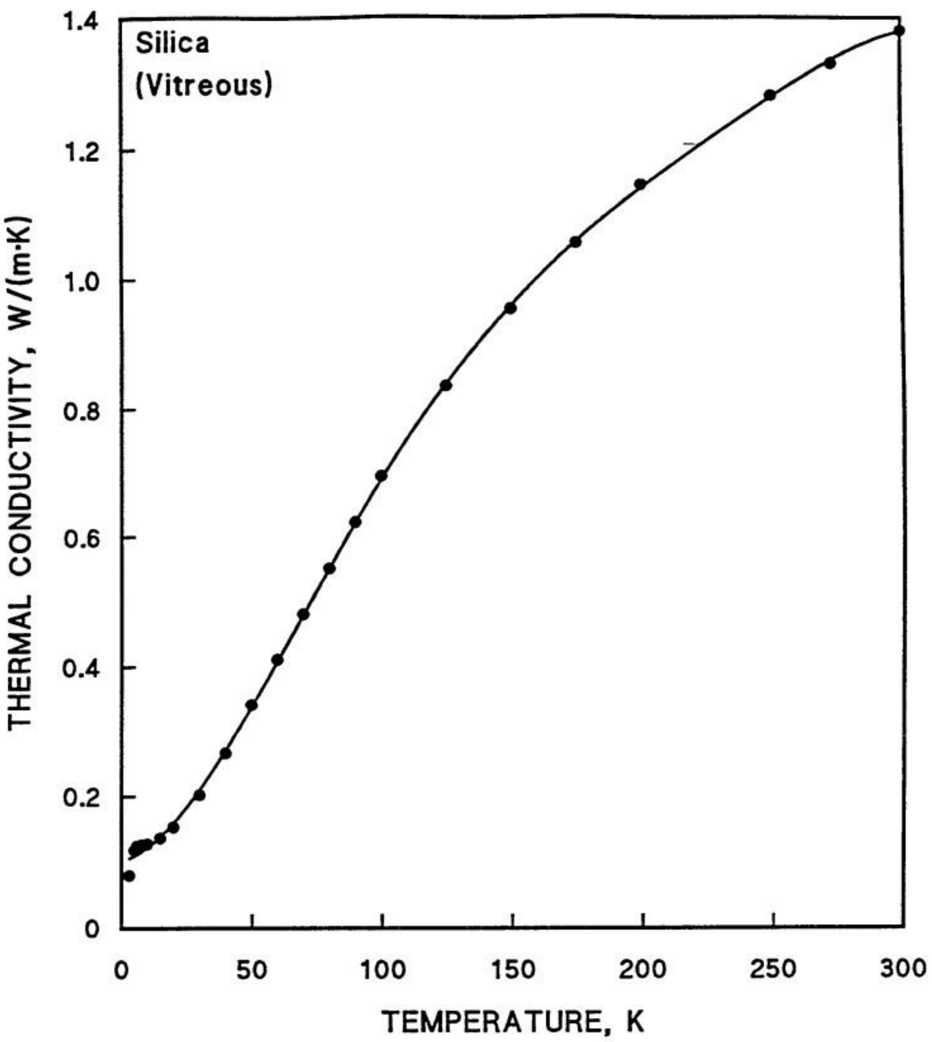
Thermal conductivity

Thermal conductivity dependance with ambient temperature can be approximated by a funcion of the type:

$$k(T) = c + a \frac{T^{\alpha}}{1 + \left(\frac{T}{b}\right)^{\beta}}$$

Curves are taken from NISTIR 5030 by J. D. Simon, Cryogenic Properties of Inorganic Insulation Materials for ITER Magnets: A Review

Fused Silica Substrate



Digitized points data (full range, Touloukian)

$T_d :=$

	0
0	3
1	5
2	...

$k_d :=$

	0
0	0.08
1	0.118
2	...

Standard function (Origin)

$A_s :=$

	0
0	$1.695 \cdot 10^{-4}$
1	105.471
2	1.907
3	1.72
4	0.107

$$k_s(T) := \left[A_{s_4} + A_{s_0} \cdot \frac{\left(T \cdot K^{-1}\right)^{A_{s_2}}}{1 + \left(\frac{T \cdot K^{-1}}{A_{s_1}}\right)^{A_{s_3}}} \right] \cdot \frac{W}{m \cdot K}$$

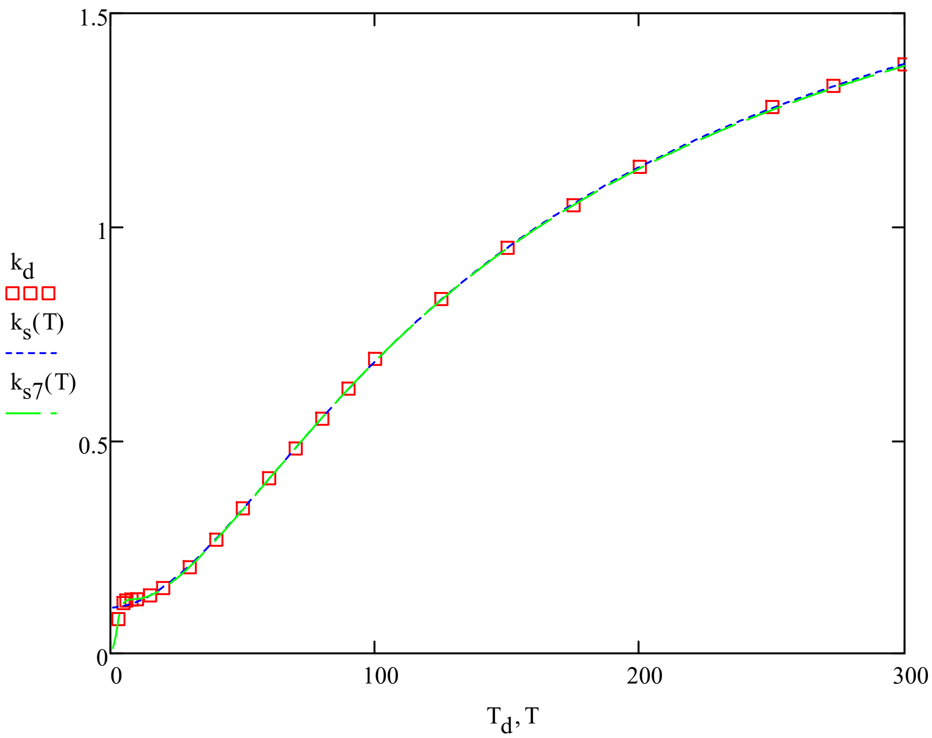
Logarithmic-Polynomial fit (Origin)

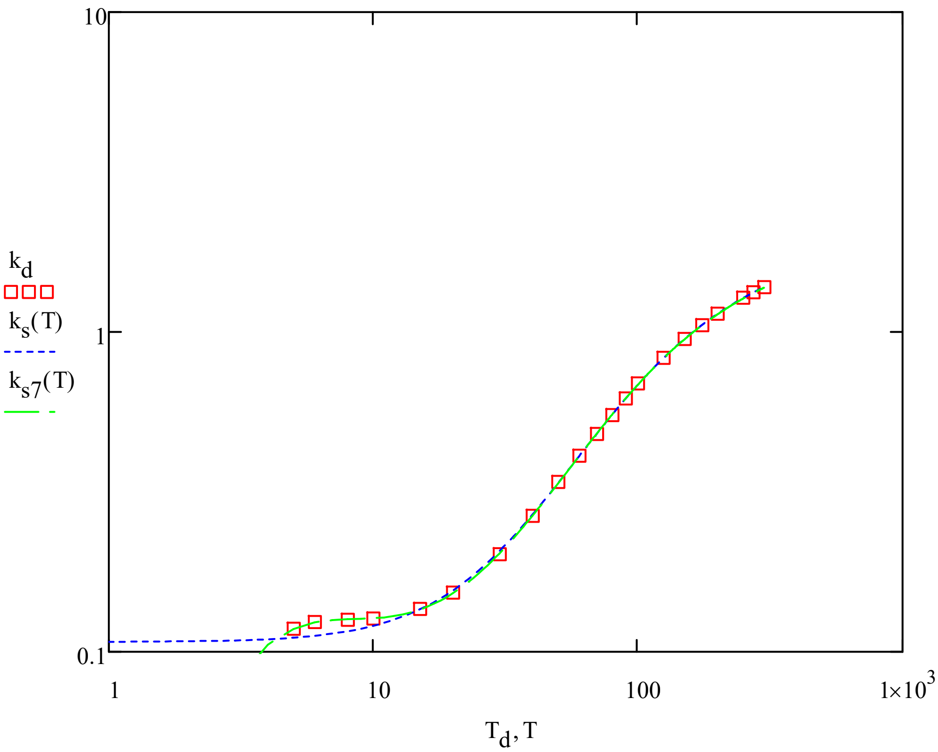
$B_s :=$

	0
0	-1.9321
1	0.6855
2	8.1525
3	-19.4883
4	18.5372
5	-8.6573
6	1.9872
7	-0.1801

$$k_{s7}(T) := 10^{\sum_{i=0}^{7} \left(B_{s_i} \cdot \log\left(T \cdot K^{-1}\right)^i\right)} \cdot \frac{W}{m \cdot K}$$

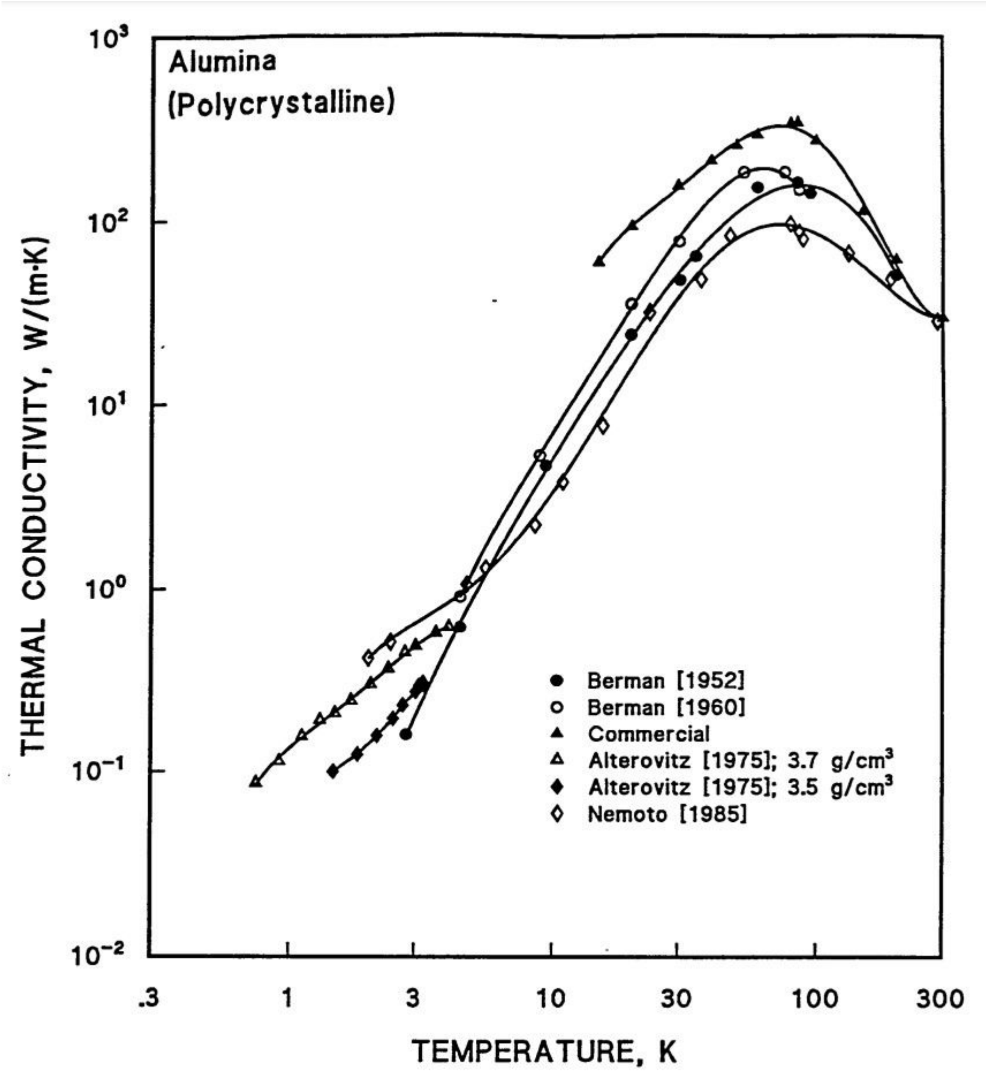
$T := 1K, 2K .. 300K$





10
1
0.1
1
10
100
1×10^3
k_d
k_s(T)
k_s7(T)
T_d, T

Alumina Substrate



Digitized points data (Nemoto)

$T_d :=$

	0
0	2.043
1	2.48
2	...

$k_d :=$

	0
0	0.423
1	0.524
2	...

Standard function (Origin)

$A_a :=$

	0
0	$6.08 \cdot 10^{-3}$
1	58.459
2	2.542
3	3.758
4	0.3

Logarithmic-Polynomial fit (Origin)

$B_e :=$

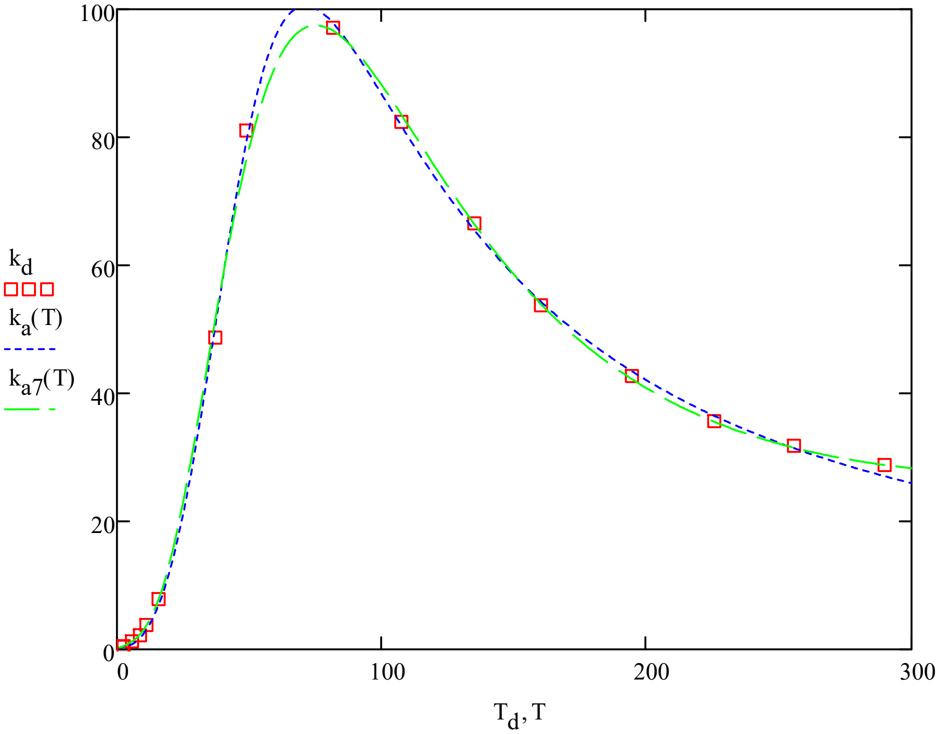
	0
0	-0.4887
1	-1.4347
2	11.0706
3	-23.6159
4	25.5901
5	-13.9004
6	3.6126

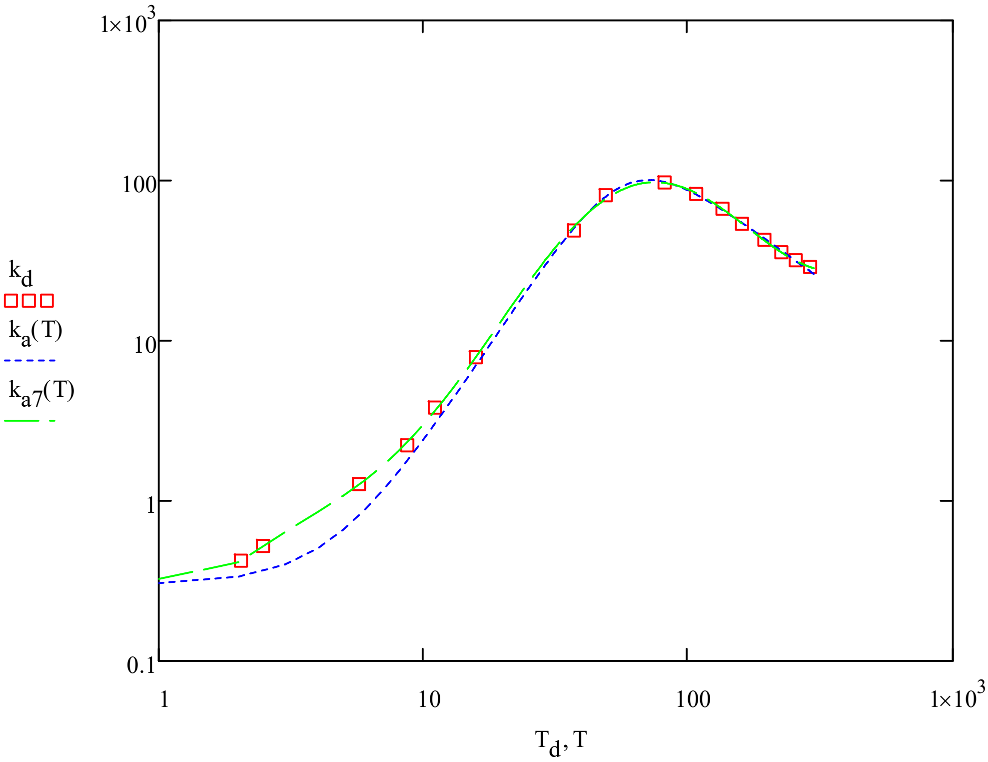
7	-0.3585

$$k_a(T) := \left[A_{a_4} + A_{a_0} \cdot \frac{\left(T \cdot K^{-1}\right)^{A_{a_2}}}{1 + \left(\frac{T \cdot K^{-1}}{A_{a_1}}\right)^{A_{a_3}}}\right] \cdot \frac{W}{m \cdot K}$$

$$k_{a7}(T) := 10^{\sum_{i=0}^{7} \left(B_{e_i} \cdot \log\left(T \cdot K^{-1}\right)^{i}\right)} \cdot \frac{W}{m \cdot K}$$

$$T := 1K, 2K .. 300K$$





Epotek H-20

Digitized points data (Amils thesis)

$T_d :=$

	0
0	3.21
1	3.345
2	...

$k_d :=$

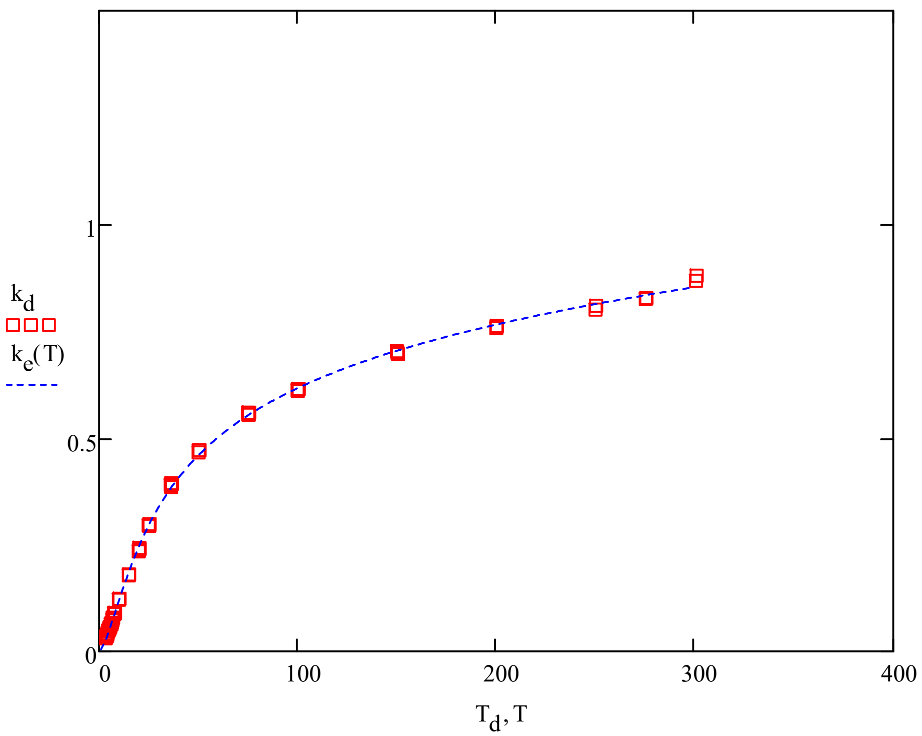
	0
0	0.031
1	0.031
2	...

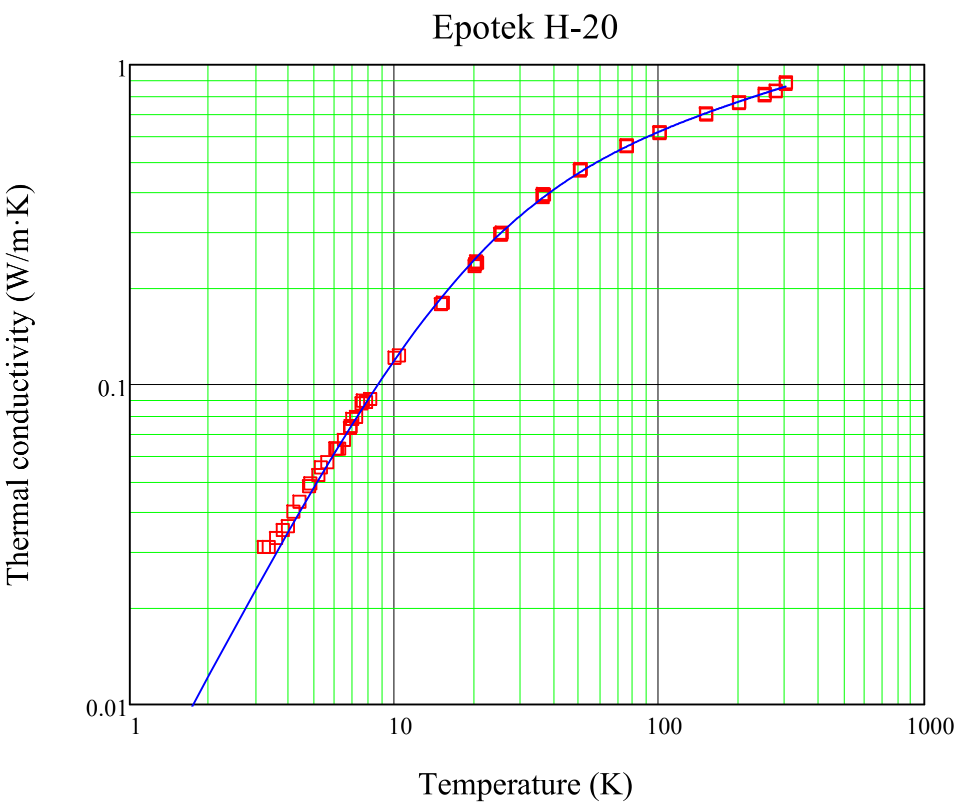
Standard function (Amils thesis)

$A_e :=$

	0
0	$4.307 \cdot 10^{-3}$
1	18.917
2	1.593
3	1.366

$$k_e(T) := A_{e_0} \cdot \frac{\left(T \cdot K^{-1}\right)^{A_{e_2}}}{1 + \left(\frac{T \cdot K^{-1}}{A_{e_1}}\right)^{A_{e_3}}} \cdot \frac{W}{m \cdot K}$$





Calculations

Resistor	Height:	$H := 10 \cdot mil$
	Area:	$A := 20 \cdot mil \cdot 10 \cdot mil$
	Value:	$R := 100 \cdot ohm$
Epoxy	Thickness:	$\delta := 10 \cdot \mu m$
Module	Temperature:	$T_0 := 12K$
	Current:	$I := 7 \cdot mA$

Initial estimation

A rough approximation considering constant thermal conductivity:

Dissipated power in the resistor: $P := I^2 \cdot R$

$$\Delta T(k) := \frac{P}{A} \cdot H \cdot \frac{1}{k}$$

Vitreous silica @12 K: $k := k_{s7}(12K)$ $\quad k = 0.129 \cdot \frac{W}{m \cdot K}$ $\quad T_f := \Delta T(k) + T_0$ $\quad T_f = 86.595\,K$

Alumina @12 K: $k := k_{a7}(12K)$ $\quad k = 4.293 \cdot \frac{W}{K \cdot m}$ $\quad T_f := \Delta T(k) + T_0$ $\quad T_f = 14.247\,K$

Second approximation

According to the Fourier law, the heat flux q in an uniform and isotropic material of thermal conductivity k:

$\vec{\Phi}_q = -k \cdot \nabla T$ for an unidimensional flux $\Phi_q = -k \cdot \frac{d}{dx} T$ (a)

The rate of variation of energy inside the material is equal to the flux of heat over the boundary surface S:

$\frac{d}{dt} E = \int \vec{\Phi}_q \, d\vec{s}$ for a uniform distribution $\Phi_q = \frac{P}{S}$ (b)

Integrating (a) y (b) from x_1 to x_2 we obtain the following expression:

$$P = \frac{S}{\Delta x} \cdot \int_{T_1}^{T_2} k(T) \, dT$$

In our case, x range is H, the heat flows only across a surface A from T_f to T_0 and the power transferred is P (we do not consider thermal radiation).

For vitreous silica:

Dado $P = \frac{A}{H} \cdot \int_{T_0}^{T_f} k_{s7}(T) \, dT$ $T_{fs} := \mathrm{Find}(T_f)$ $T_{fs} = 54.02\,K$

For alumina:

Dado $P = \frac{A}{H} \cdot \int_{T_0}^{T_f} k_{a7}(T) \, dT$ $T_{fa} := \mathrm{Find}(T_f)$ $T_{fa} = 13.904\,K$

Epoxy contribution

We consider now a layer of δ thickness of Epotek H-20 underneath the base of the resistor:

Dado $P = \frac{A}{\delta} \cdot \int_{T_0}^{T_f} k_e(T) \, dT$ $T_e := \mathrm{Find}(T_f)$ $T_e = 14.338\,K$

For vitreous silica:

Dado $P = \frac{A}{H} \cdot \int_{T_e}^{T_f} k_{s7}(T) \, dT$ $T_{fs} := \mathrm{Find}(T_f)$ $T_{fs} = 54.853\,K$

For alumina:

Dado $P = \frac{A}{H} \cdot \int_{T_e}^{T_f} k_{a7}(T) \, dT$ $T_{fa} := \mathrm{Find}(T_f)$ $T_{fa} = 15.708\,K$

Current and Power - Temperature plots

Fused silica

Resistor	Height:	$H := 10 \cdot mil$
	Area:	$A := 20 \cdot mil \cdot 10 \cdot mil$
	Value:	$R := 50 \cdot ohm$
Epoxy	Thickness:	$\delta := 10 \cdot \mu m$
Module	Temperature:	$T_0 := 14K$
	Current:	$I := 0 \cdot mA, 0.5 \cdot mA .. 20 \cdot mA$

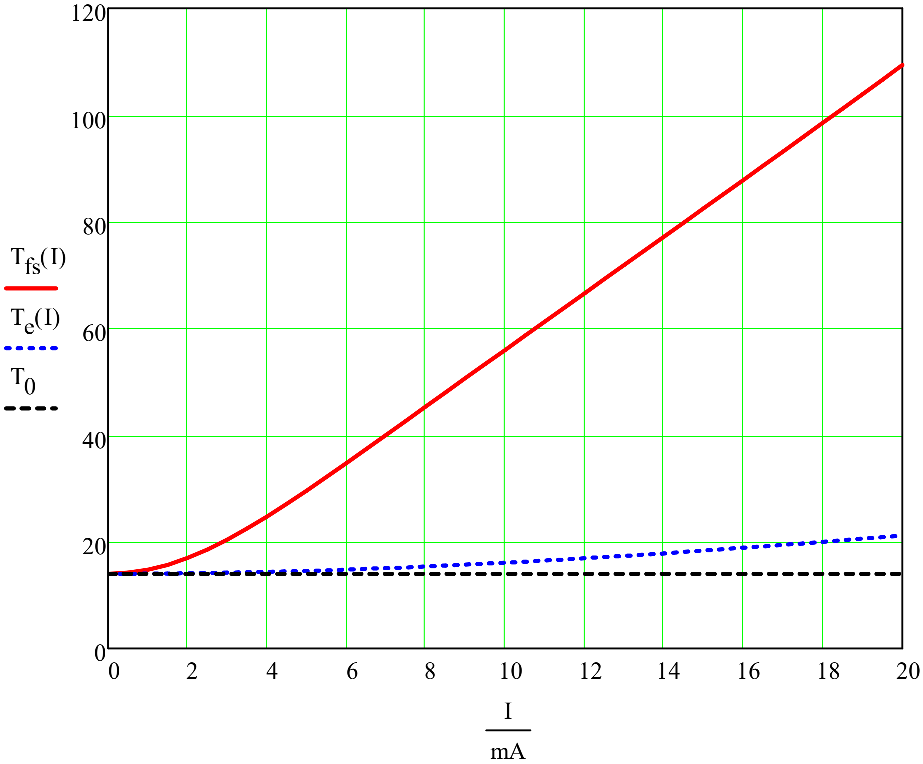
$P(I) := I^2 \cdot R$ $\qquad Pd(I) := \frac{P(I)}{A}$

Initial guess: $T_e := T_0 + 5K$ $\qquad T_{fs} := T_e + 40K$

$$T_e(I) := \mathrm{root}\left(P(I) - \frac{A}{\delta} \cdot \int_{T_0}^{T_e} k_e(T)\, dT, T_e\right)$$

$$T_{fs}(I) := \mathrm{root}\left(P(I) - \frac{A}{H} \cdot \int_{T_e(I)}^{T_{fs}} k_{s7}(T)\, dT, T_{fs}\right)$$

k_{sc7} from cryogenic range only curve (Zeller and Pohl) is less pessimistic (less heating). Use only below 60 K.



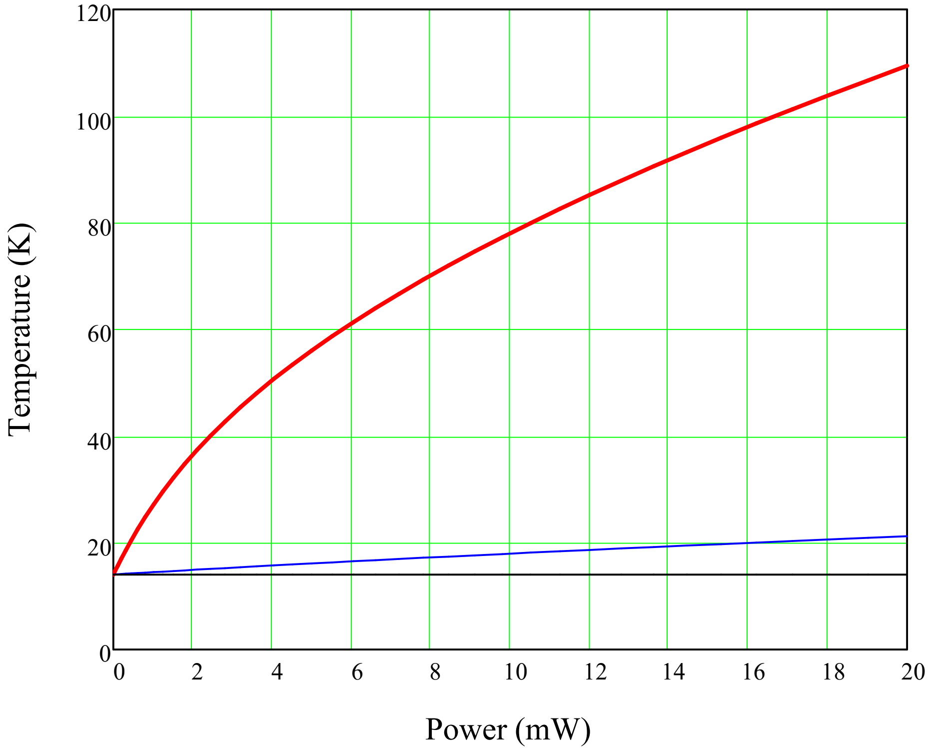
$T_{fs}(I) =$

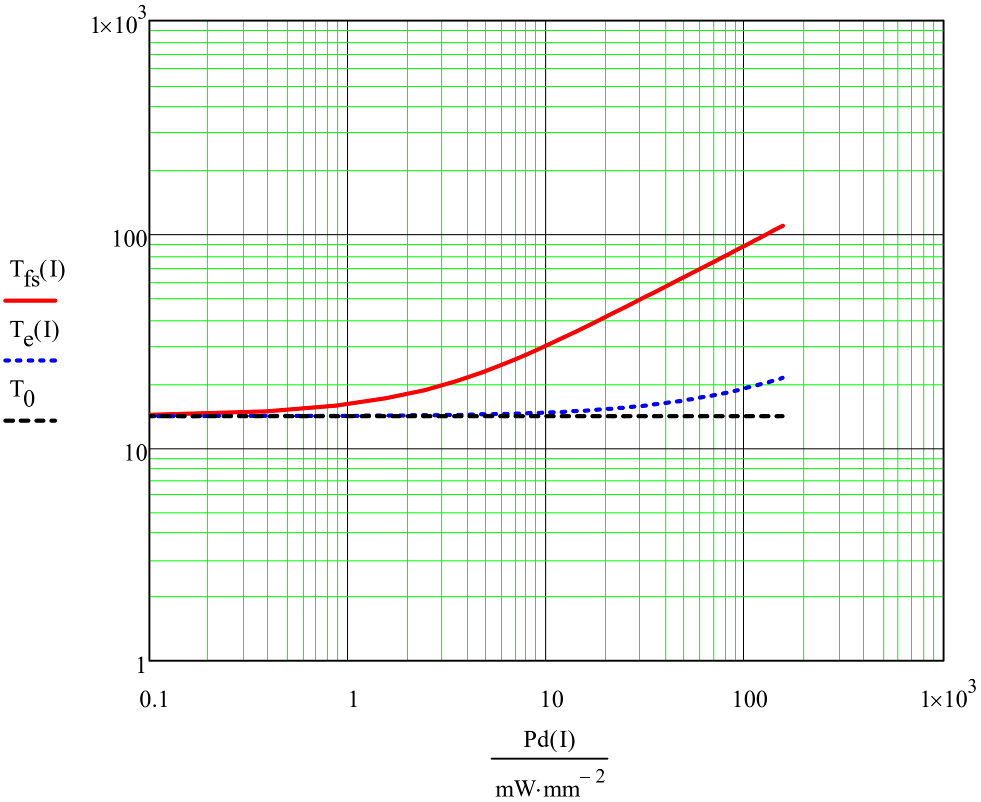
14	K
14.19	
14.757	
15.688	
16.962	
18.545	
20.397	
22.472	
24.723	
27.107	
29.59	
32.142	
34.741	
37.371	
40.02	
...	

$I =$

0	·m
0.5	
1	
1.5	
2	
2.5	
3	
3.5	
4	
4.5	
5	
5.5	
6	
6.5	
7	
...	

10 mils Quartz 0102 + 10 μm Epotek H-20 @14 K





Alumina

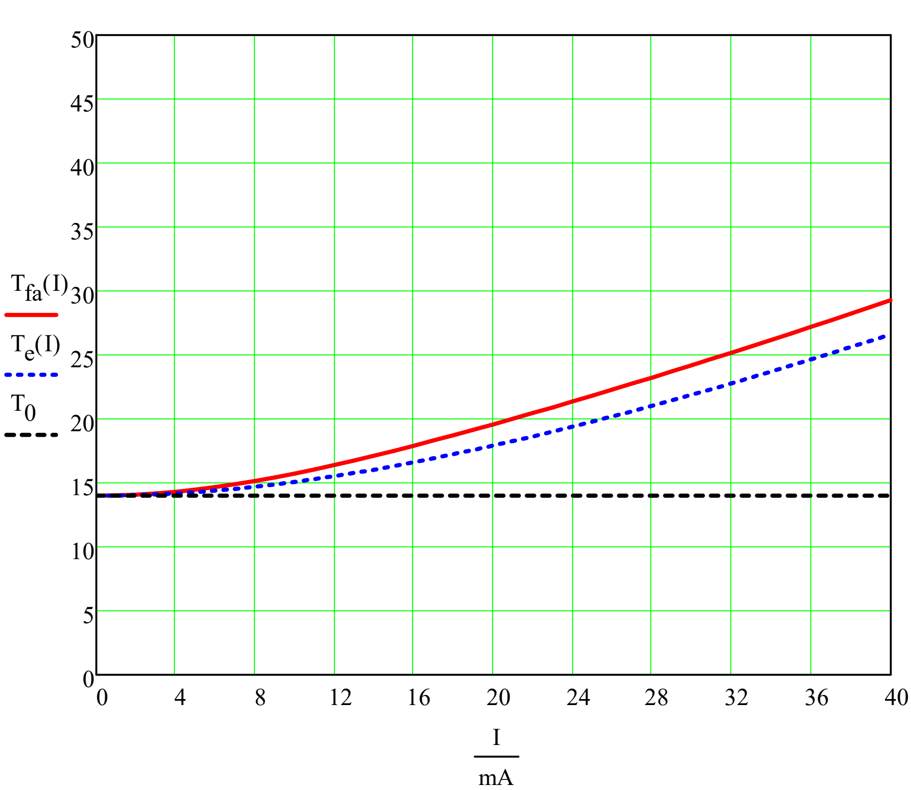
Resistor	Height:	$H := 10 \cdot mil$
	Area:	$A := 20 \cdot mil \cdot 20 \cdot mil$
	Value:	$R := 50 \cdot ohm$
Epoxy	Thickness:	$\delta := 10 \cdot \mu m$
Module	Temperature:	$T_0 := 14 \cdot K$
	Current	$I := 0 \cdot mA, 1 \cdot mA .. 40 \cdot mA$

$P(I) := I^2 \cdot R$ $\qquad Pd(I) := \frac{P(I)}{A}$

Initial guess: $T_e := T_0 + 5K$ $\qquad T_{fa} := T_e + 20K$

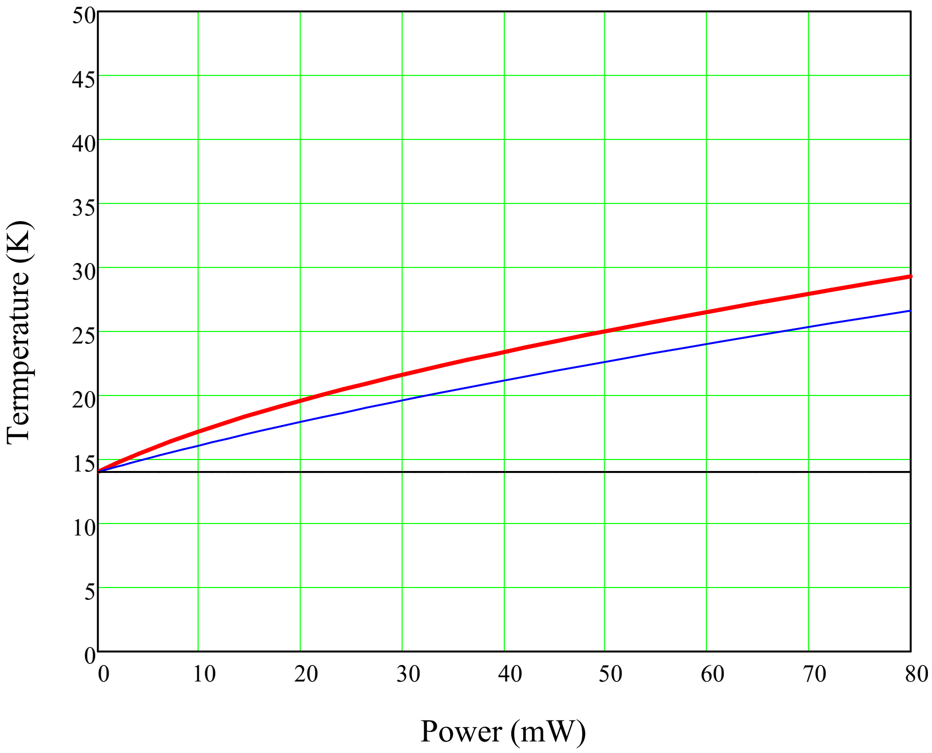
$$T_e(I) := root\left(P(I) - \frac{A}{\delta} \cdot \int_{T_0}^{T_e} k_e(T)\, dT, T_e\right)$$

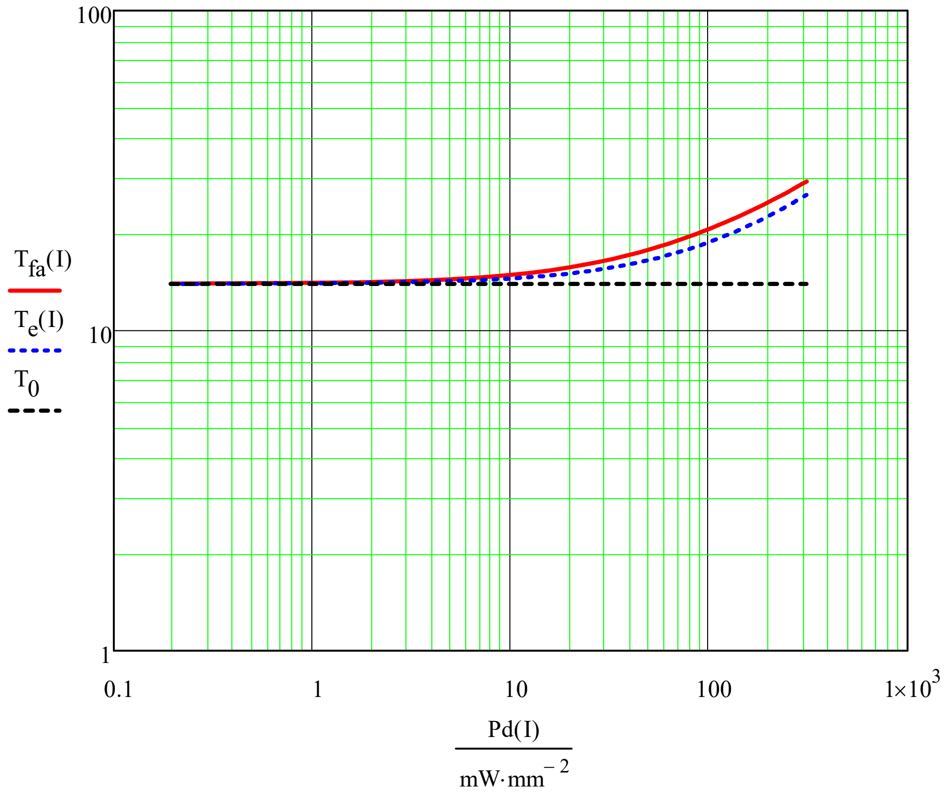
$$T_{fa}(I) := root\left(P(I) - \frac{A}{H} \cdot \int_{T_e(I)}^{T_{fa}} k_{a7}(T)\, dT, T_{fa}\right)$$



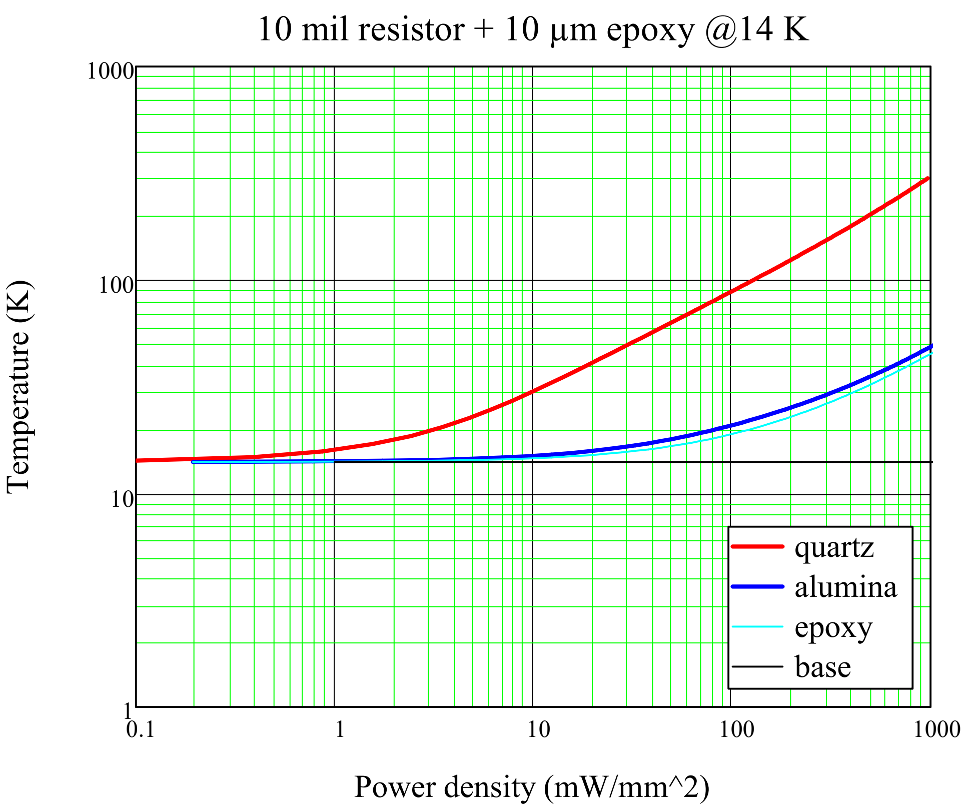
$T_{fa}(I)$ =		I =	
14	K	0	·mA
14.019		1	
14.077		2	
14.172		3	
14.304		4	
14.47		5	
14.668		6	
14.896		7	
15.152		8	
15.432		9	
15.735		10	
16.058		11	
16.399		12	
16.756		13	
17.128		14	
...		...	

10 mils Alumina 0202 + 25 µm Epotek H-20 @14 K





Comparison (power density)



Noise Temperature of Quartz Resistor Biased

Determined by noise power measurements at a fixed frequency with the resistor biased (on) and unbiased (off)

$$Tsys = Tamp + \frac{Tnfm}{Gamp}$$

System noise temperature (known) (amplifier + Noise Figure Meter)

$$Y = \frac{Pon}{Poff}$$

Y factor of resistor with/without bias (measured)

$$Tsys = \frac{Th - Y \cdot Tc}{Y - 1}$$

Tsys and Tc are known and Y is measured. Th can be calculated as:

$$Th = Tc \cdot Y - Tsys + Tsys \cdot Y \qquad Th = Tc \cdot \frac{Pon}{Poff} - Tsys + Tsys \cdot \frac{Pon}{Poff}$$

$$Th = \frac{Pon}{Poff} \cdot (Tc + Tsys) - Tsys \qquad Th = (Tc + Tsys) \cdot 10^{\frac{(Pon\_dB - Poff\_dB)}{10}} - Tsys$$

Example :

$$Gamp(Gamp\_dB) := 10^{\left(\frac{Gamp\_dB}{10}\right)}$$

$$Th(Pon\_dB, Poff\_dB, Tc, Tsys) := (Tc + Tsys) \cdot 10^{\frac{(Pon\_dB - Poff\_dB)}{10}} - Tsys$$

Change the values in green for the calculation .

$Tamp := 6.18$ $\quad Tnfm := 1386.21$ $\quad Gamp\_dB := 37.98$ $\quad Tc := 13.79$

$Poff\_dB := 26.06$ $\quad Pon\_dB := 33.33$

$$Tsys := Tamp + \frac{Tnfm}{Gamp(Gamp\_dB)} \qquad Tsys = 6.401$$

$Th(Pon\_dB, Poff\_dB, Tc, Tsys) = 101.283$ Result : noise temperature of biased resistor

Building a table of Temperature vs Power

The source current is the parameter controlled to simplify the power calculation. This avoids accounting for voltage drop in the cables.

COMPEX QUARTZ 0102 @ 15 K

$Rl := 50$ Resistor value in Ohm

$Area := 10 \cdot mil 20 \cdot mil$

$Area = 0.129\,mm^2$

$$P\_mW(I\_mA) := \left(\frac{I\_mA}{1000}\right)^2 \cdot Rl \cdot 1000$$

Power in mW

$I\_mA :=$

	0
0	0
1	1
2	2
3	5
4	7
5	10
6	15
7	20

$$P\_mW(I\_mA) = \begin{pmatrix} 0 \\ 0.05 \\ 0.2 \\ 1.25 \\ 2.45 \\ 5 \\ 11.25 \\ 20 \end{pmatrix}$$

$Poff\_dB = 26.06$

$Pon\_dB :=$

	0
0	26.06
1	26.25
2	26.72
3	28.57
4	29.54
5	30.76
6	32.21
7	33.34

$$Th(Pon\_dB, Poff\_dB, Tc, Tsys) = \begin{pmatrix} 13.79 \\ 14.693 \\ 17.104 \\ 29.587 \\ 38.593 \\ 53.186 \\ 76.805 \\ 101.532 \end{pmatrix}$$

Variables for the graph

$P\_qu := P\_mW(I\_mA)$

$Th\_qu := Th(Pon\_dB, Poff\_dB, Tc, Tsys)$

$$Ps\_qu := \frac{P\_qu}{Area \cdot mm^{-2}}$$

Ps_qu is power (mW) per mm2 of surface

SOTA ALUMINA 0102 @ 15 K

$Rl := 50$ Resistor value in Ohm

$Area := 20 \cdot mil 20 \cdot mil$

$Area = 0.258\,mm^2$

$$P\_mW(I\_mA) := \left(\frac{I\_mA}{1000}\right)^2 \cdot Rl \cdot 1000$$

Power in mW

$I\_mA :=$

	0
0	0
1	1
2	2
3	5
4	7
5	10
6	15
7	20
8	25
9	30
10	35
11	40

$P\_mW(I\_mA) =$

	0
0	0
1	0.05
2	0.2
3	1.25
4	2.45
5	5
6	11.25
7	20
8	31.25
9	45
10	61.25
11	80

$Poff\_dB = 26.06$

$Pon\_dB :=$

	0
0	26.07
1	26.09
2	26.12
3	26.35
4	26.57
5	26.93
6	27.52
7	28.05
8	28.53
9	28.98
10	29.39
11	29.76

$Th(Pon\_dB, Poff\_dB, Tc, Tsys) =$

	0
0	13.837
1	13.93
2	14.071
3	15.184
4	16.306
5	18.268
6	21.858
7	25.526
8	29.257
9	33.15
10	37.065
11	40.931

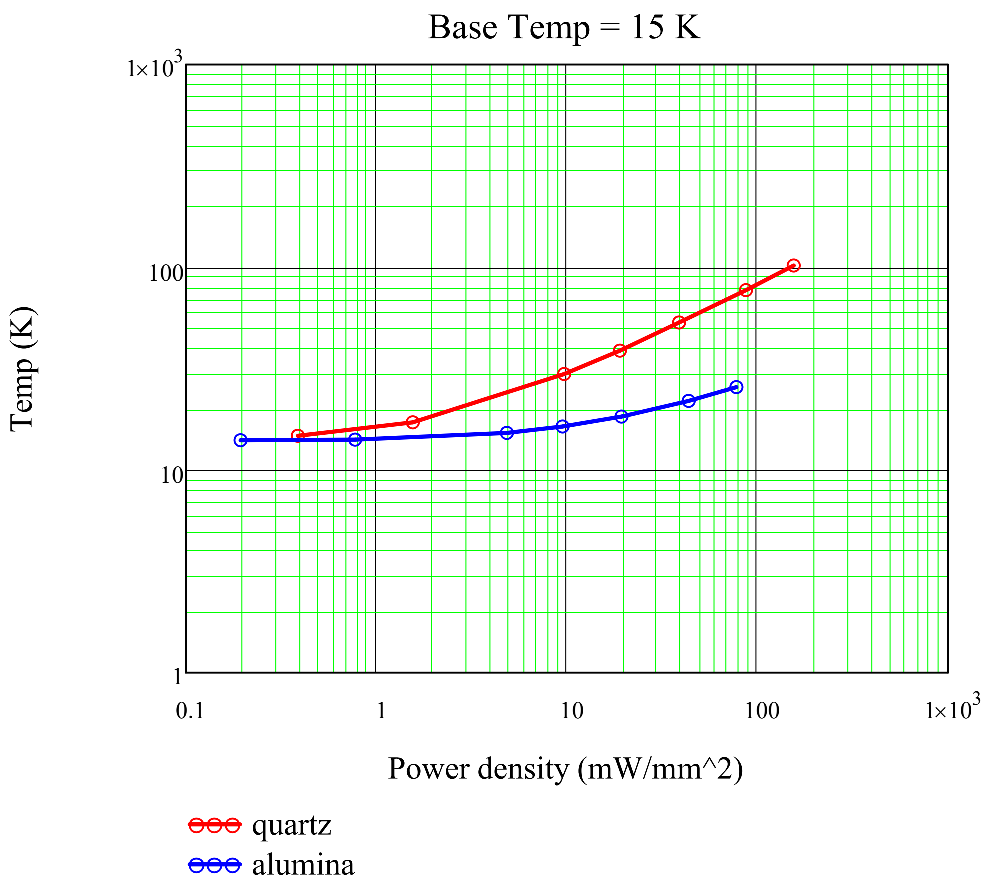
Variables for the graph

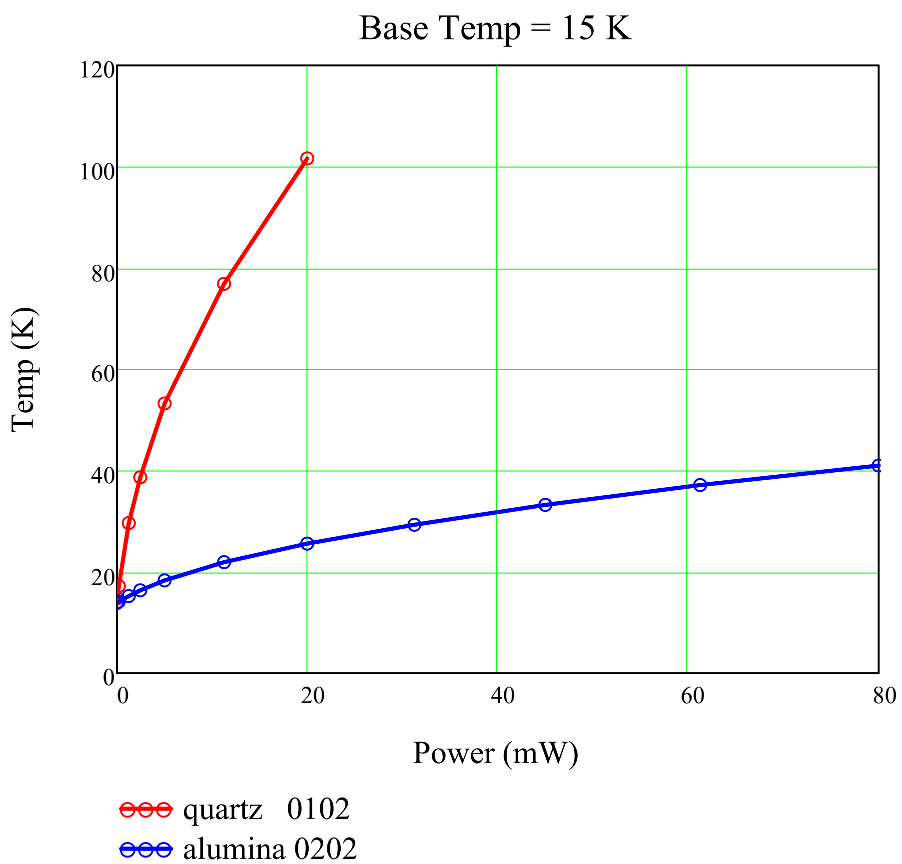
$P\_al := P\_mW(I\_mA)$

$Th\_al := Th(Pon\_dB, Poff\_dB, Tc, Tsys)$

$$Ps\_al := \frac{P\_qu}{Area \cdot mm^{-2}}$$

Ps_qu is power (mW) per mm2 of surface


Base Temp = 15 K
Temp (K)
Power density (mW/mm^2)
1×10^3
100
10
1
0.1
1
10
100
1×10^3
quartz
alumina


Base Temp = 15 K
Temp (K)
Power (mW)
120
100
80
60
40
20
0
0
20
40
60
80
quartz 0102
alumina 0202