SiGe microwave cryogenic low noise amplifier design YSG1

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1. Introduction

YSG series 1 are 0.1 - 1.1 GHz low noise cryogenic amplifiers designed and built at the *Observatorio de Yebes* for the Purple Mountain Observatory SIS receivers. They are based on the wider band design YSG 0. A short description of YSG0 LNA is included in Appendix I.

2. Amplifier development

The main specifications of the amplifier were:

- Frequency band: 0.1 1.1 GHz
- Input/Output Reflection: < 15 dB
- Average gain: > 35 dB
- Average noise temperature: Best effort

2.1 Prototype modification

The first stage of the new amplifier development was to modify the existing YSG0 design to meet the specifications, with especial attention to the lower end of the frequency band. These modifications, which included new components and changes in some component values changes, were modelled with ADS and tested in two existing YSG0 prototypes. One of these prototypes was further modified to have and independent bias voltage for each stage. This simplifies the interpretation of results and allows more flexibility in the optimization. The different modifications and test results are mentioned bellow.

Inter-stage coupling capacitor

Different capacitor values have been tested in order to improve the performance in the 0.1-1.1 GHz band. The noise and gain measurements are shown in Figure 2, where it can be seen that a higher capacitance improves the behaviour at low frequencies.

The value of the interstage capacitor finally used was 22 pF.



Figure 1: Noise Figure Meter measurements with different inter-stage capacitors



First stage collector inductor and output resistor

In order to improve the reflection in the band, some changes were performed. The combined results are shown in figure 2:

- The input reflection decreased changing the first stage collector SMD inductor of 3 nH by a 100 nH inductance made with AWG 36 gold plated wire (14 turns of 1 mm in diameter, 2 mm long). This inductance was changed later by a SMD inductor of 100 nH (0603), more repetitive and easier to mount.
- The output resistor of 51 Ω was also changed by a 10 Ω one, achieving a better output and also input reflection.



Figure 2: Inductor and output resistor effect

One side-effect of these changes was the non unconditional stability of the amplifier: the Rollet factor was lower than 1 at 8 GHz at cryogenic temperature.

RC circuit and ferrite toroid

In order to solve the stability problem an RC circuit from the second stage collector to ground was added. The values calculated with ADS, were 20 Ω for the resistor (the available value used was 22.6 Ω) and 1 pF for the capacitor.

Although a decrease of gain at high frequencies was achieved, the Rollet factor did not improve as expected at 8 GHz with the RC circuit (see figure 3).

An alternative solution to improve the stability was to mount a ferrite toroid around a wire between the first stage collector and the inter-stage capacitor. A reduction of both reflections and gain was achieved and therefore, an improvement of the Rollet factor. Several tests with different positions and orientations of the toroid, different toroid sizes and materials and different lengths, number of turns and types of wire were performed. It was found that the better option was a toroid as described in figure 4 crossed by 1 turn of enameled wire. The result of the improvement is shown in figure 5. \bigotimes



Figure 3: RC circuit at output effect. Note that despite the unconditional stability at room temperature, the Rollet factor always decreases upon cooling and it was lower than 1 at 8 GHz at cryogenic temperature.



Micrometals toroid	T-10-1
Inner diameter	1.12 mm
Outer diameter	2.46 mm
Height	0.76 mm
Nominal Inductance	3.2 nH/N ²

Figure 4: Photograph and characteristics of the mounted toroid



Figure 5: Toroid effect. Only results with the toroid and wire finally used are shown

Transistor

Different models of commercially available packaged NPN SiGe transistors with good noise performance were tested in the first stage of one prototype to compare their cryogenic noise temperature. The tested transistors were BFU725 from NXP and BFP720 and BFP840ESD from Infineon. Infineon transistors have lower power consumption than NXP. BFP840ESD has an ESD protection circuit. The results are shown in figure 6. BFP720 transistor was probably oscillating, as it had a positive input reflection coefficient at 11 GHz and the noise temperature was abnormally high. The best results were obtained with the transistor of the original design (NXP BFU725F/N1), which was chosen for the final version.



Figure 6: Transistor comparison

Other modifications

⋘

Other minor changes carried out with respect to YSG0 were:

- The base resistor of both stages was changed from 1.5 k Ω to 1k Ω in order to improve slightly the input and output reflection
- A slight improvement of the stability was achieved removing the 2.2 pF capacitor at the output

Figure 7 shows the final schematic of the amplifier.



Figure 7: YSG1 amplifier final schematic



2.2 Chassis and substrate design

The design of the substrate has been made trying to keep it as compact as possible while observing the necessary restrictions for its assembly. It has been fabricated in a Rogers RT Duroid 6002 with a thickness of 5 mils.

The modifications with respect to YSG0 are listed below:

- Bigger coil in the first stage (from 0402 to 0603)
- Recess in the substrate to insert the ferrite toroid
- RC circuit at the second stage collector
- Transistors in orthogonal orientation

The amplifier chassis is made of gold plated aluminum.

The DC bias connector is a 2-pin PCB socket connector with 2 mm pitch from Preci-Dip (Ref. 830-80-002-40-001101). After some tests to optimize the bias of each stage independently in the prototype, and in view of the little improvement obtained, it was decided to maintain only one bias voltage for both stages.

Input and output RF ports are SMA female connectors from Radial (Ref. R125-460-000).



Figure 8: YSG1 amplifier substrate

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	COMPONENTES											
CODE	VALUE	MNFR	P/N									
R1-R4	10.2	TE CONNECTIVITY	CPF0402B10R2E1									
R5-R6	102	TE CONNECTIVITY	CPF0402B102RE1									
R7-R8	1K02	TE CONNECTIVITY	CPF0402B1K02E1									
R9	22.6	TE CONNECTIVITY	CPF0402B22R6E1									
C1-C4	470p	AVX	04025A471JAT2A									
C5	22p	AVX	04025A220JAT2A									
C6	1p	AVX	04025U1R0BAT2A									
C7	2p2	AVX	04023J2R2BBSTR									
C8	1n	AVX	06035A102JAT2A									
L1	100n	MURATA	LPW18ANR10J00D									
Q1-Q2		NXP	BFU725F/N1 (2014)									
D1		NEXPERIA	BZX384-C5∨1									
T1		MICROMETALS	⊤10−1									

Figure 9: List of components of YSG1 amplifier

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	DC CONNECTOR							
	PIN	SI GNAL						
[1	GND						
-[2	VC						











Figure 10: YSG1 mechanical and electrical interface, external dimensions and DC connector pin-out



Figure 11: Internal view of YSG 1002 amplifier



Figure 12: External view of YSG 1002 amplifier

3. Measurements

Noise temperature (and gain) was measured with a system based on a computer controlled Agilent N8975A Noise Figure Meter described in detail in [1], [2]. Room temperature data were obtained with an Agilent N4000A noise diode. The DUT is cooled in a Dewar with a CTI 1020 refrigerator. Cryogenic measurements were taken with the "cold attenuator" method, using an Agilent N4002A noise diode (at room temperature) plus a 15 dB attenuator and a Heat-Block device cooled at cryogenic temperature. Temperature is carefully monitored in the attenuator body using a Lake Shore sensor diode. An absolute accuracy (@ 2 σ) of 14 K at T_{amb}=297 K and 1.7 K at T_{amb}=14 K can be estimated with methods presented in [3]. Repeatability is better than these values by an order of magnitude.



S parameters were measured in the same Dewar with an Agilent E8364B Vector Network Analyzer from 0.1 to 20.1 GHz. A detailed description of the measurement procedure used at cryogenic temperature can be found in [1], [2]. The amplifier output is connected to one of the stainless steel Dewar transitions and its input to the other through a semi-flexible Cu cable. A full two port calibration is done at room temperature with the electronic calibration kit Agilent N4693-60001 inside the Dewar in place of the amplifier, with the same semi-flexible cable. The stainless steel lines are supposed to be invariant with temperature. The Cu cable is measured at cryogenic temperature independently and its loss is taken into account to correct S11 and S21. Time domain gating is used to correct for the residual reflection changes in the lines.

Additional measurements to ensure the absence of oscillations were performed at room and cryogenic temperatures.

4. Results

Four amplifiers were assembled and tested with similar results. The data of them is presented in figures 13, 14 and 15. Table 1 shows a summary of the measurements at cryogenic temperature. The datasheets of the three amplifiers sent to Purple Mountain Observatory are presented in [4].



Figure 13: Measurement of return loss of YSG amplifiers at cryogenic temperature

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Figure 14: Measurement of gain and noise temperature of YSG amplifiers at cryogenic temperature



Figure 15: Measurement of Rollet factor of YSG amplifiers at cryogenic temperature

	YSG1 0.1-1-1 GHz amplifiers @ 15 K											
Amplifier	T_{nmean}	$_{mean} T_{n min} G_{mean} / \Delta G S11_{max} $				K _{min}						
ID	(K)	(K)	(dB)	(dB)	(dB)							
YSG 1001	7.1	6.2	42.6/2.23	-14.4	-16.2	1.65						
YSG 1002	6.9	6.1	42.3/2.35	-13.4	-16.2	1.68						
YSG 1003	7.1	6.4	42.6/2.38	-13.6	-16.1	1.65						
YSG 1004	6.8	6	42.6/2.24	-14.3	-16.2	1.68						

Table 1: Summary of measurements of YSG1 amplifiers at cryogenic temperature



Appendix I: YSG0 LNA design

This LNA is based on a Caltech design (S. Weinreb, 2008) [5]. It has two stages of SiGe HBT transistors (model NXP BFU725F/N1) that work in a common emitter configuration. Only one bias voltage is required to bias the amplifier, as seen in Figure 16.



Figure 16: YSG0 amplifier schematic



Figure 17: External view of an YSG0 LNA

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Figure 18: YSG0 amplifier substrate

	COMPONENTES											
CDDE	VALUE	MNFR	P/N									
R1-R3	10	VISHAY	CRCW040210R0FKED									
R4-R5	100	VISHAY	CRCW0402100RFKED									
R6	1K5	VISHAY	CRCW04021K50FKED									
R7	1K	VISHAY	CRCW04021K00FKED									
R8	51	VISHAY	CRCW040251R0FKED									
C1-C4	470p	AVX	04025A471JAT2A									
C5-C6	2p2	AVX	04023J2R2BBSTR									
C7	1n	AVX	06035A102JAT2A									
L1	3n	MURATA	LQP15MN3N0W02D									
Q1-Q2		NXP	BFU725F/N1 (2014)									
D1		NEXPERIA	BZX384-C5∨1									

Figure 19: List of components of YSG0 amplifier

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Noise and gain results of YSGO design at cryogenic temperature for two different frequency bands are presented in Figure 20.



Figure 20: Noise and gain measurement of a YSG0 LNA at 15 K



Appendix II: Datasheets



Type CPF Series

Key Features

Thin film precision resistors with TC's to 15ppm and tolerances to 0.05%.

Wide range of case sizes from 0201 to 2512

Suitable for all applications where close accuracy and stability are essential

Terminal finish – electroplated 100% matte Sn

Applications

Communications

Industrial Controls

Instrumentation

Medical



The CPF series is a high stability precision chip resistor range offering various power dissipations relating to a wide range of chip sizes. The CPF series offers TCR's down to 15ppm/°C and resistance tolerances to 0.1%. Standard values are within the IEC 63 E96 and E24 value grids. The CPF has accurate and uniform physical dimensions to facilitate placement

Electrical Characteristics

Chip Size		0201					
Rated Power @70°C		0.03125W					
Pasistance Pango O	Min.	49R9	49R9	49R9	49R9		
Resistance Range Ω	Max	4K99	33K	4K99	33K		
Tolerance		0.	5		1		
Code Letter		D			F		
Selection series			E24 & E96				
Temp. Coefficient (ppm/°C)		25	50	25	50		
Code Letter		E	С	E	С		
Operating Voltage (Max)		15V					
Max. Overload Voltage		30V					
Operating Temp. Range	-55 ~ +155°C						
Insulation Resistance dry min.	>1000MΩ						
Stability	0.5%						

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Dimensions in millimetres unless otherwise specified Dimensions Shown for reference purposes only. Specifications subject to change



Chip Size		0402											
Rated Power @70	0.063W												
Resistance	Min. 49R9		49R9	10)R	49R9	4R7		49R9	4	R7		
Range Ω	Max		20K		69K8	25	5K	69K8	51	1K	69K8	51	.1K
Tolerance (%)		0.05 0.1						0.5		1			
Code Letter	А				В			D			F		
Selection series		E24 & E96											
T.C.R. (ppm/°C)		15	25	50	15	25	50	15	25	50	15	25	50
Code Letter		D	E	С	D	E	С	D	E	С	D	E	С
Max Operating Vo	olt.	25V											
Max. Overload Vo	olt.						50	VC					
Op. Temp. Range							-55 ~ -	+155°C					
Insulation Resista	>1000MΩ												
Stability							0.	5%					

Chip Size		0603											
Rated Power @70	0.063W												
Resistance	Min.		4R7		4R7	4	R7	4R7	1R0		4R7	1R0	
Range Ω	Max		332K		511K	11	V 0	511K	11	v10	511K	11	V 0
Tolerance (%)			0.05		0.1			0.5			1		
Code Letter		А		В			D			F			
Selection series		E24 & E96											
T.C.R. (ppm/°C)		15	25	50	15	25	50	15	25	50	15	25	50
Code Letter		D	E	С	D	E	С	D	E	С	D	E	С
Max Operating Vo	olt.	50V											
Max. Overload Vo	lt.						10	0V					
Op. Temp. Range		-55 ~ +155°C											
Insulation Resista	nce	>1000ΜΩ											
Stability							0.	5%					

Chip Size		0805												
Rated Power @70	0.1W													
Resistance	Min.		4R7		4R7	4	R7	4R7	1R0		4R7	11	R0	
Range Ω	Max		1M0		1M0	21	V 0	1M0	21	<i>/</i> 10	1M0	21	/ 0	
Tolerance (%)			0.05		0.1				0.5			1		
Code Letter	А			В			D			F				
Selection series		E24 & E96												
T.C.R. (ppm/°C)		15	25	50	15	25	50	15	25	50	15	25	50	
Code Letter		D	E	С	D	E	С	D	E	С	D	E	С	
Max Operating Vo	olt.	100V												
Max. Overload Vo	lt.						20	00V						
Op. Temp. Range	-55 ~ +155°C													
Insulation Resista	>1000MΩ													
Stability							0.	5%						

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Dimensions in millimetres unless otherwise specified Dimensions Shown for reference purposes only. Specifications subject to change



Derating Curve



Construction and dimensions



1	Alumina Substrate	4	Edge Electrode (NiCr)	Ø	Resistor Layer (NiCr)
2	Bottom Electrode (Ag)	5	Barrier Layer (Ni)	8	Overcoat (Epoxy)
3	Top Electrode (Ag)	6	External Electrode (Sn)	9	Marking

Size	L (mm)	W (mm)	T (mm)	D1 (mm)	D2 (mm)	Weight (g)
						(1000 Pcs.)
0201	0.58±0.05	0.29±0.05	0.23±0.05	0.12±0.05	0.15±0.05	0.14
0402	1.00±0.05	0.50±0.05	0.30±0.05	0.20±0.10	0.20±0.10	0.54
0603	1.55±0.10	0.80±0.10	0.45±0.10	0.30±0.20	0.30±0.20	1.83
0805	2.00±0.15	1.25±0.15	0.55±0.10	0.30±0.20	0.40±0.20	4.71
1206	3.05±0.15	1.55±0.15	0.55±0.10	0.42±0.20	0.35±0.25	9.02
1210	3.10±0.15	2.40±0.15	0.55±0.10	0.40±0.20	0.55±0.25	10
2010	4.90±0.15	2.40±0.15	0.55±0.10	0.60±0.30	0.50±0.25	23.61
2512	6.30±0.15	3.10±0.15	0.55±0.10	0.60±0.30	0.50±0.25	38.06



Recommended Land Pattern										
Size	A	В	С							
0201	0.25	0.30	0.40±0.2							
0402	0.50	0.50	0.60±0.2							
0603	0.80	1.00	0.90±0.2							
0805	1.00	1.00	1.35±0.2							
1206	2.00	1.15	1.70±0.2							
1210	2.00	1.15	2.50±0.2							
2010	3.60	1.40	2.50±0.2							
2512	4.90	1.60	3.10±0.2							

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Dimensions in millimetres unless otherwise specified Dimensions Shown for reference purposes only. Specifications subject to change



Reflow Solder Profile



Time of Reflow soldering at maximum temperature point 260°C = 10s

Wave Solder Profile



Time of Wave soldering at maximum temperature point 260°C = 10s

Time of Soldering Iron at maximum temperature point 410°C = 5s

How To Order

CPF	0603		0603		B 100R		E	1
Common Part	Package Size		Tolerance	Value	TCR	Packaging		
CPF - precision	0201	1206	B - ±0.1%	100R - 100Ω	D – 15PPM	1 – 1K REEL		
thin film chip	0402	1210	D - ±0.5%	1KO - 1000Ω	E - 25PPM	Blank – standard reel		
resistor	0603 2010		F - ±1%	10K – 10,000Ω	C - 50PPM	0201 0402 - 10K		
	0805	2512				0603 0805 1206 1210 – 5K		
						2010 2512 - 4K		

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Dimensions in millimetres unless otherwise specified Dimensions Shown for reference purposes only. Specifications subject to change

COG (NP0) Dielectric



RoHS COMPLIANT

General Specifications



C0G (NP0) is the most popular formulation of the

"temperature-compensating," EIA Class I ceramic materials. Modern C0G (NP0) formulations contain neodymium, samarium and other rare earth oxides.

COG (NP0) ceramics offer one of the most stable capacitor dielectrics available. Capacitance change with temperature is 0 ±30ppm/°C which is less than ±0.3% C from -55°C to +125°C. Capacitance drift or hysteresis for COG (NP0) ceramics is negligible at less than ±0.05% versus up to ±2% for films. Typical capacitance change with life is less than ±0.1% for COG (NP0), one-fifth that shown by most other dielectrics. COG (NP0) formulations show no aging characteristics.

PART NUMBER (see page 2 for complete part number explanation)



NOTE: Contact factory for availability of Termination and Tolerance Options for Specific Part Numbers. Contact factory for non-specified capacitance values.











Variation of Impedance with Ceramic Formulation Impedance vs. Frequency 1000 pF - C0G (NP0) vs X7R



C0G (NP0) Dielectric



Specifications and Test Methods

Parameter/Test		NP0 Specification Limits	Measuring Conditions				
Operating Tempera	ature Range	-55°C to +125°C	Temperature Cycle Chamber				
Capaci	tance	Within specified tolerance	Freg.: 1.0 MHz ± 10	% for cap ≤ 1000 pF			
		<30 pF: Q≥ 400+20 x Cap Value	1.0 kHz ± 10% fo	or cap > 1000 pF			
	Q	≥30 pF: Q≥ 1000	Voltage: 1.0)Vrms ± .2V			
Insulation Re	sistance	100,000MΩ or 1000MΩ - μF,	Charge device with	n rated voltage for			
		WHICHEVELIS IESS	but ± 5 secs @ room temp/humidity				
Dielectric S	strength	No breakdown or visual defects	1-5 seconds, w/charge limited to 50 Note: Charge device voltage for 50	Charge device with 250% of rated voltage for 1-5 seconds, w/charge and discharge current limited to 50 mA (max) Note: Charge device with 150% of rated voltage for 500V devices.			
	Appearance	No defects	Deflectio	on: 2mm			
Resistance to	Capacitance Variation	$\pm 5\%$ or $\pm .5$ pF, whichever is greater		∇ 1mm/sec			
Flexure	Q	Meets Initial Values (As Above)		V			
Silesses	Insulation Resistance	≥ Initial Value x 0.3					
Solder	ability	≥ 95% of each terminal should be covered with fresh solder	Dip device in eutectic for 5.0	solder at 230 ± 5ºC ± 0.5 seconds			
	Appearance	No defects, <25% leaching of either end terminal					
	Capacitance Variation	\leq ±2.5% or ±.25 pF, whichever is greater	Din dovice in outoetic e	Idor at 260%C for 60sec			
Resistance to Solder Heat	Q	Meets Initial Values (As Above)	onds. Store at room ten	nperature for 24 ± 2hours			
	Insulation Resistance	Meets Initial Values (As Above)	before measuring electrical properties.				
	Dielectric Strength	Meets Initial Values (As Above)					
	Appearance	No visual defects	Step 1: -55°C ± 2°	30 ± 3 minutes			
	Capacitance Variation	\leq ±2.5% or ±.25 pF, whichever is greater	Step 2: Room Temp	≤ 3 minutes			
Thermal	Q	Meets Initial Values (As Above)	Step 3: +125°C ± 2° 30 ± 3 minutes				
Snock	Insulation Resistance	Meets Initial Values (As Above)	Step 4: Room Temp	≤ 3 minutes			
	Dielectric Strength	Meets Initial Values (As Above)	Repeat for 5 cycles 24 hours at roo	and measure after om temperature			
	Appearance	No visual defects					
	Capacitance Variation	$\leq \pm 3.0\%$ or $\pm .3$ pF, whichever is greater	Charge device with t	wice rated voltage in			
Load Life	Q (C=Nominal Cap)	≥ 30 pF: Q≥ 350 ≥10 pF, <30 pF: Q≥ 275 +5C/2 <10 pF: Q≥ 200 +10C	test chamber se for 1000 hou	t at 125°C ± 2°C urs (+48, -0).			
	Insulation Resistance	≥ Initial Value x 0.3 (See Above)	room temperatu	amber and stabilize at ure for 24 hours easuring			
	Dielectric Strength	Meets Initial Values (As Above)		g.			
	Appearance	No visual defects					
	Capacitance Variation	$\leq \pm 5.0\%$ or $\pm .5$ pF, whichever is greater	Ctars in a test shamb	a_{1} and a_{2} B_{2}^{0} C_{1} C_{2}^{0}			
Load Humidity	Q	≥ 30 pF: Q≥ 350 ≥10 pF, <30 pF: Q≥ 275 +5C/2 <10 pF: Q≥ 200 +10C	Store in a test chamb 85% ± 5% relative hu (+48, -0) with rate	imidity for 1000 hours d voltage applied.			
	Insulation Resistance	≥ Initial Value x 0.3 (See Above)	Remove from chamber temperature for 24 ± 2 h	r and stabilize at room ours before measuring.			
	Dielectric Strength	Meets Initial Values (As Above)					



COG (NP0) Dielectric



Capacitance Range

PREFERRED SIZES ARE SHADED

			-		-		-															
SIZI	E	0101*	0201		0402	2			0603			0805				1206						
Solde	ring	Reflow Only	Reflow Or	ly	Reflow/Wa	ave	Reflow/Wave			Reflow/Wave				Reflow/Wave								
Packa	ging	All Paper	All Pape	r	All Pape	r			All Pape	er			Pap	er/Embo	ssed				Paper/E	mbossed		
L) Length	mm (in.)	0.40 ± 0.02 (0.016 ± 0.0008)	0.60 ± 0.0 (0.024 ± 0.0	09 04)	1.00 ± 0 (0.040 ±	0.10 0.004)		(0	1.60 ± 0. 0.063 ± 0.0	.15 006)		2.01 ± 0.20 (0.079 ± 0.008)				3.20 ± 0.20 (0.126 ± 0.008)						
W) Width	mm	0.20 ± 0.02	0.30 ± 0.0)	0.50 ± 0	0.10			0.81 ± 0.1	15		1.25 ± 0.20				1.60 ± 0.20						
t) Terminal	(in.) mm	(0.008 ± 0.0008) 0.10 + 0.04	(0.011 ± 0.0	04)	(0.020 ± 0.25 ± 0	0.004)).15		(0.	032 ± 0.0	06) 15			(0.	.049 ± 0.0	008) 25		(0.063 ± 0.008)					
ty reminar	(in.)	(0.004 ± 0.0016)	(0.006 ± 0.0	02)	(0.010 ±	0.006)		(0.	.014 ± 0.0	06)			(0	.020 ± 0.0	010)				(0.020	± 0.20 ± 0.010)		
0.55	WVDC	16	25 5) 16	25	50	16	25	50	100	200	16	25	50	100	200	16	25	50	100	200	500
(pF)	1.0	В	A A		c	C C	G	G	G	G		J	J	J	J	J	J	J	J	J	J	J
	1.2	В	A A	C	С	C	G	G	G	G		J	J	J	J	J	J	J	J	J	J	J
	1.5	B	A A A				G	G	G	G		J	J	J	J	J	J	J	J	J	J	J
	2.2	В	A A	С	С	С	G	G	G	G		J	J	J	J	J	J	J	J	J	J	J
	2.7	B	A A	C	C C	C	G	G	G	G		J	J	J	J	J	J	J	J	J	J	J
	3.3	B	A A	C C	c	C C	G	G	G	G		J	J	J	J	J	J	J	J	J	J	J
	4.7	В	A A	с	С	С	G	G	G	G		J	J	J	J	J	J	J	J	J	J	J
	5.6 6.8	В			C C		G	G	G	G		J	J	J	J	J	J	J	J	J	J	J
	8.2	B	A A	C	С	c	G	G	G	G		J	J	J	J	J	J	J	J	J	J	J
	10	В	A A	С	С	С	G	G	G	G	G	J	J	J	J	J	J	J	J	J	J	J
	12	B	A A		c	C C	G	G	G	G	G	J	J	J	J	J	J	J	J	J	J	J
	18	В	A A	С	С	С	G	G	G	G	G	J	J	J	J	J	J	J	J	J	J	J
	22 27	B	A A A		c	C C	G	G	GG	G	G	J	J	J	J	J	J	J	J	J	J J	J
	33	В	A A	C	С	С	G	G	G	G	G	J	J	J	J	J	J	J	J	J	J	J
	39	B		C	C	C	G	G	G	G	G	J	J	J	J	J	J	J	J	J	J	J
	56	B	A A	C	C	C	G	G	G	G	G	J	J	J	J	J	J	J	J	J	J	J
	68	В	A A	C	C	C	G	G	G	G	G	J	J	J	J	J	J	J	J	J	J	J
	100	B	A A		C C	C C	G	G	G	G	G	J	J	J	J	J	J	J	J	J	J	J
	120			c	С	c	G	G	G	G	G	J	J	J	J	J	J	J	J	J	J	J
	150			C	С С	C C	G	G	G	G	G	J	J	J	J	J	J	J	J	J	J	J
	220			c	c	c	G	G	G	G	G	J	J	J	J	J	J	J	J	J	J	M
	270			С	C	C	G	G	G	G		J	J	J	J	J	J	J	J	J	J	M
	390				C C	C C	G	G	G	G		J	J	J	J	J	J	J	J	J	J	M
	470			С	C	C	G	G	G	G		J	J	J	J	J	J	J	J	J	J	M
	560 680				C C	C C	G	G	G	G		J	J	J	J	J	J	J	J	J	J	M P
	820			c	С	С	G	G	G	G		J	J	J	J	J	J	J	J	J	М	
	1000 1200			С	С	C	G	G	G	G		J	J	J	J	J	J	J	J	J	Q Q	
	1500						G	G	G			J	J	J	J		J	J	J	M	Q	
	1800						G	G	G			J	J	J	N		J	J	M	М	Q	
	2200						G	G	G			N	N	N	N		J	J	M	P	Q	
	3300						G	G	G			Р	Р	Р	N		J	J	M	Р	Q	
	3900 4700						G	G	G			P	P P	P	N		J	J	M	P		
	5600				1	1						Р	Р	Р			J	J	М	Р		
	6800 8200		\sim		~-w-							P	P P	P P			M	M	M	P P		
Сар	0.010	<u> </u>		\frown	7	\leq						Р	Р	Р			P	P	P	Р		
(µF)	0.012		(-			Ł																
	0.015			\mathbf{P}																		
	0.022			t																		
	0.027																					
	0.039																					
	0.047																					
	0.082																					
	0.1	10	25 5	<u> </u>			10	05	50	400	0000	10	05	50	10.5	0000	10	05		400	0000	F.0.2
SIZI		16 0101*	25 50 0201	16	0402	50	16	25	0603	100	200	16	25	0805	100	200	16	25	50	100 206	200	500
0121	-		5201		0402				0000									_	12		_	
Letter Max		A B	C 0.5	3	E 0.71	G 0.90	(J).94	K		M 1.27	N)	P 1.52	Q	8	X	2	Y .54	Z 2.79	-	
Thickness	(0	0.013) (0.009	9) (0.02	2) (0.028)	(0.035)	(0	.037)	(0.040) ((0.050)	(0.05	5)	(0.060)	(0.0)	70)	(0.090)	(0.	100)	(0.110)		
L				PAPER	2		_							EMB	OSSEI	D						

PAPER and EMBOSSED available for 01005



RF/Microwave C0G (NP0) Capacitors (RoHS)

Ultra Low ESR, "U" Series, C0G (NP0) Chip Capacitors

GENERAL INFORMATION

"U" Series capacitors are COG (NP0) chip capacitors specially designed for "Ultra" low ESR for applications in the communications market. Max ESR and effective capacitance

DIMENSIONS: inches (millimeters)

 $\frac{1}{B} \begin{bmatrix} t & A & -t \\ B & t & C \\ t & t \end{bmatrix}$

0402



0603



0805

1210.



are met on each value producing lot to lot uniformity. Sizes available are EIA chip sizes 0402, 0603, 0805, and

inches (mm)

Size	Α	В	С	D	E
0402	0.039±0.004 (1.00±0.1)	0.020±0.004 (0.50±0.1)	0.022 (0.55mm) max	N/A	N/A
0603	0.060±0.010 (1.52±0.25)	0.030±0.010 (0.76±0.25)	0.036 (0.91mm) max	0.010±0.005 (0.25±0.13)	0.030 (0.76) min
0805	0.079±0.008 (2.01±0.2)	0.049±0.008 (1.25±0.2)	0.040±0.005 (1.02±0.127)	0.020±0.010 (0.51±0.255)	0.020 (0.51) min
1210	0.126±0.008 (3.2±0.2)	0.098±0.008 (2.49±0.2)	0.050±0.005 (1.27±0.127)	0.025±0.015 (0.635±0.381)	0.040 (1.02) min

HOW TO ORDER



ELECTRICAL CHARACTERISTICS

Capacitance Values and Tolerances:

Size 0402 - 0.2 pF to 30 pF @ 1 MHz Size 0603 - 1.0 pF to 100 pF @ 1 MHz Size 0805 - 1.6 pF to 160 pF @ 1 MHz Size 1210 - 2.4 pF to 1000 pF @ 1 MHz

Temperature Coefficient of Capacitance (TC):

0±30 ppm/°C (-55° to +125°C)

Insulation Resistance (IR):

 $10^{12}~\Omega$ min. @ 25°C and rated WVDC $10^{11}~\Omega$ min. @ 125°C and rated WVDC

Working Voltage (WVDC):

<u> </u>		<u> </u>	,	
Size		Working	Voltage	
0402	-	100, 50	, 25 WVDC	
0603	-	200, 10), 50 WVDC	;
0805	-	200, 10	D WVDC	

1210 - 200, 100 WVDC

ance Options for Specific Part Numbers.

Dielectric Working Voltage (DWV):

250% of rated WVDC

Equivalent Series Resistance Typical (ESR):

- 0402 See Performance Curve, page 9
- 0603 See Performance Curve, page 9
- 0805 See Performance Curve, page 9
- 1210 See Performance Curve, page 9
- Marking: Laser marking EIA J marking standard (except 0603) (capacitance code and tolerance upon request).

MILITARY SPECIFICATIONS

Meets or exceeds the requirements of MIL-C-55681

RF/Microwave C0G (NP0) Capacitors (RoHS)

Ultra Low ESR, "U" Series, C0G (NP0) Chip Capacitors

CAPACITANCE RANGE



ULTRA LOW ESR, "U" SERIES



TYPICAL ESR vs. FREQUENCY

Frequency (MHz)





TYPICAL ESR vs. FREQUENCY 0603 "U" SERIES



TYPICAL ESR vs. FREQUENCY 1210 "U" SERIES



ESR Measured on the Boonton 34A

RF/Microwave C0G (NP0) Capacitors

Ultra Low ESR, "U" Series, C0G (NP0) Chip Capacitors



Frequency (GHz)

muRata Inductor Data Sheet





< List of part numbers with package codes >

LQW18ANR10J00D , LQW18ANR10J00J , LQW18ANR10J00B





•

Packaging code	Specifications	Minimum quantity
D	φ180mm Paper taping	4000
J	φ330mm Paper taping	10000
В	Packing in bulk	500

Mass (Typ.)	
1 piece	0.003g

Specifications

Inductance	100nH ±5%
Inductance test frequency	100MHz
Rated current (Itemp) (Based on Temperature rise)	220mA
Max. of DC resistance	0.68Ω
Q (min.)	34
Q test frequency	150MHz
Self resonance frequency (min.)	1800MHz
Operating temperature range (Self-temperature rise is not included)	-55~125°C
Series	LQW18AN_00

🔔 Attention

1. This datasheet is downloaded from the website of Murata Manufacturing Co., Ltd. Therefore, it's specifications are subject to change or our products in it may be discontinued

without advance notice. Please check with our sales representatives or product engineers before ordering.

2. This datasheet has only typical specifications because there is no space for detailed specifications.

Therefore, please review our product specifications or consult the approval sheet for product specifications before ordering.



Chart of characteristic data (The charts below may show another part number which shares its characteristics.)





🔔 Attention

This datasheet is downloaded from the website of Murata Manufacturing Co., Ltd. Therefore, it's specifications are subject to change or our products in it may be discontinued without advance notice. Please check with our sales representatives or product engineers before ordering.
 This datasheet has only typical specifications because there is no space for detailed specifications.

Therefore, please review our product specifications or consult the approval sheet for product specifications before ordering.

NPN wideband silicon germanium RF transistor

Rev. 2 — 3 November 2011

Product data sheet

1. Product profile

1.1 General description

NPN silicon germanium microwave transistor for high speed, low noise applications in a plastic, 4-pin dual-emitter SOT343F package.

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A or equivalent standards.

1.2 Features and benefits

- Low noise high gain microwave transistor
- Noise figure (NF) = 0.7 dB at 5.8 GHz
- High maximum stable gain 27 dB at 1.8 GHz
- 110 GHz f_T silicon germanium technology

1.3 Applications

- 2nd LNA stage and mixer stage in DBS LNB's
- Satellite radio
- Low noise amplifiers for microwave communications systems
- WLAN and CDMA applications
- Analog/digital cordless applications
- Ka band oscillators (DRO's)

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V_{CBO}	collector-base voltage	open emitter		-	-	10	V
V_{CEO}	collector-emitter voltage	open base		-	-	2.8	V
V _{EBO}	emitter-base voltage	open collector		-	-	1.0	V
I _C	collector current			-	25	40	mA
P _{tot}	total power dissipation	$T_{sp} \le 90 \ ^{\circ}C$	<u>[1]</u>	-	-	136	mW
h _{FE}	DC current gain	I _C = 10 mA; V _{CE} = 2 V; T _i = 25 °C		160	280	400	



NPN wideband silicon germanium RF transistor

Table 1.	Quick reference data	continued				
Symbol	Parameter	Conditions	Min	Тур	Мах	Unit
C_{CBS}	collector-base capacitance	V _{CB} = 2 V; f = 1 MHz	-	70	-	fF
f _T	transition frequency	I _C = 25 mA; V _{CE} = 2 V; f = 2 GHz; T _{amb} = 25 °C	-	55	-	GHz
G _{p(max)}	maximum power gain	I _C = 25 mA; V _{CE} = 2 V; f = 5.8 GHz; T _{amb} = 25 °C	[2] _	18	-	dB
NF	noise figure	I _C = 5 mA; V _{CE} = 2 V; f = 5.8 GHz; Γ _S = Γ _{opt} ; T _{amb} = 25 °C	-	0.7	-	dB

[1] T_{sp} is the temperature at the solder point of the emitter lead.

[2] $G_{p(max)}$ is the maximum power gain, if K > 1. If K < 1 then $G_{p(max)}$ = Maximum Stable Gain (MSG).

2. Pinning information

Table 2.	Discrete pinning		
Pin	Description	Simplified outline	Graphic symbol
1	emitter		
2	base		4
3	emitter		2
4	collector		1.3
			mbb159

3. Ordering information

Table 3. Ordering information								
Type number	Package	Package						
	Name	Description	Version					
BFU725F/N1	-	plastic surface-mounted flat pack package; reverse pinning; 4 leads	SOT343F					

4. Marking

Table 4. Marking			
Type number	Marking	Description	
BFU725F/N1	B7*	* = p : made in Hong Kong	
		* = t : made in Malaysia	
		* = W : made in China	

BFU725F_N1 Product data sheet

NPN wideband silicon germanium RF transistor

5. Limiting values

Table 5. In accordan	able 5. Limiting values							
Symbol	Parameter	Conditions	Min	Max	Unit			
V _{CBO}	collector-base voltage	open emitter	-	10	V			
V _{CEO}	collector-emitter voltage	open base	-	2.8	V			
V _{EBO}	emitter-base voltage	open collector	-	1.0	V			
I _C	collector current		-	40	mA			
P _{tot}	total power dissipation	$T_{sp} \le 90 \ ^{\circ}C$	<u>[1]</u> _	136	mW			
T _{stg}	storage temperature		-65	+150	°C			
Tj	junction temperature		-	150	°C			

[1] T_{sp} is the temperature at the solder point of the emitter lead.

6. Thermal characteristics

Table 6.	Thermal characteristics			
Symbol	Parameter	Conditions	Тур	Unit
R _{th(j-sp)}	thermal resistance from junction to solder point		440	K/W



NPN wideband silicon germanium RF transistor

7. Characteristics

Table 7.	Characteristics
T - 05 00 .	unloss athermulas an asifind

$I_j = 25 ^{\circ} \text{C}$	uniess otherwise specified.			_		
Symbol	Parameter	Conditions	Min	Тур	Мах	Unit
V _{(BR)CBO}	collector-base breakdown voltage	$I_{C} = 2.5 \ \mu A; I_{E} = 0 \ mA$	10	-	-	V
V _{(BR)CEO}	collector-emitter breakdown voltage	I _C = 1 mA; I _B = 0 mA	2.8	-	-	V
I _C	collector current		-	25	40	mA
I _{CBO}	collector-base cut-off current	I _E = 0 mA; V _{CB} = 4.5 V	-	-	100	nA
h _{FE}	DC current gain	I _C = 10 mA; V _{CE} = 2 V	160	280	400	
C _{CES}	collector-emitter capacitance	V _{CB} = 2 V; f = 1 MHz	-	268	-	fF
C _{EBS}	emitter-base capacitance	V _{EB} = 0.5 V; f = 1 MHz	-	400	-	fF
C _{CBS}	collector-base capacitance	V _{CB} = 2 V; f = 1 MHz	-	70	-	fF
f _T	transition frequency	I_C = 25 mA; V_{CE} = 2 V; f = 2 GHz; T_{amb} = 25 °C	-	55	-	GHz
G _{p(max)}	maximum power gain	I_C = 25 mA; V_{CE} = 2 V; T_{amb} = 25 °C	<u>[1]</u>			
		f = 1.5 GHz	-	28	-	dB
		f = 1.8 GHz	-	27	-	dB
		f = 2.4 GHz	-	25.5	-	dB
		f = 5.8 GHz	-	18	-	dB
		f = 12 GHz	- 13 -		-	dB
$ s_{21} ^2$	insertion power gain	I_C = 25 mA; V_{CE} = 2 V; T_{amb} = 25 °C				
		f = 1.5 GHz	-	26.7	-	dB
		f = 1.8 GHz	-	25.4	-	dB
		f = 2.4 GHz	-	23	-	dB
		f = 5.8 GHz	-	16	-	dB
		f = 12 GHz	-	9.3	-	dB
NF	noise figure	I_C = 5 mA; V_{CE} = 2 V; Γ_S = Γ_{opt} ; T_{amb} = 25 °C				
		f = 1.5 GHz	-	0.42	-	dB
		f = 1.8 GHz	-	0.43	-	dB
		f = 2.4 GHz	-	0.47	-	dB
		f = 5.8 GHz	-	0.7	-	dB
		f = 12 GHz	-	1.1	-	dB
G _{ass}	associated gain	I_C = 5 mA; V_{CE} = 2 V; Γ_S = Γ_{opt} ; T_{amb} = 25 °C				
		f = 1.5 GHz	-	24	-	dB
		f = 1.8 GHz	-	22	-	dB
		f = 2.4 GHz	-	20	-	dB
		f = 5.8 GHz	-	13.5	-	dB
		f = 12 GHz	-	10	-	dB

NPN wideband silicon germanium RF transistor

Table 7. T _j = 25 ℃	Characteristics continued Cunless otherwise specified.					
Symbol	Parameter	Conditions	Min	Тур	Мах	Unit
P _{L(1dB)}	output power at 1 dB gain	I_C = 25 mA; V_CE = 2 V; Z_S = Z_L = 50 Ω ; T _{amb} = 25 °C				
	compression	f = 1.5 GHz	-	8.5	-	dBm
		f = 1.8 GHz	-	9	-	dBm
		f = 2.4 GHz	-	8.5	-	dBm
		f = 5.8 GHz	-	8	-	dBm
IP3	third-order intercept point	I _C = 25 mA; V _{CE} = 2 V; Z _S = Z _L = 50 Ω; T _{amb} = 25 °C; f ₂ = f ₁ + 1 MHz				
		f ₁ = 1.5 GHz	-	17	-	dBm
		f ₁ = 1.8 GHz	-	17	-	dBm
		f ₁ = 2.4 GHz	-	17	-	dBm
		f ₁ = 5.8 GHz	-	19	-	dBm

[1] $G_{p(max)}$ is the maximum power gain, if K > 1. If K < 1 then $G_{p(max)}$ = MSG.



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BFU725F_N1

NXP Semiconductors

BFU725F/N1

NPN wideband silicon germanium RF transistor



BFU725F_N1 Product data sheet

6 of 12

NXP Semiconductors

BFU725F/N1

NPN wideband silicon germanium RF transistor



NPN wideband silicon germanium RF transistor

8. Package outline



Fig 11. Package outline SOT343F

information	provided in	this (document	is	subject	to	legal	disclaim	ers.

BFU725F_N1

All



BZX384 series Voltage regulator diodes Rev. 3 – 11 October 2016

Product data sheet

1. Product profile

1.1 General description

Low-power voltage regulator diodes in a small SOD323 (SC-76) Surface-Mounted Device (SMD) plastic package.

The diodes are available in the normalized E24 \pm 2 % (BZX384-B) and approximately ±5 % (BZX384-C) tolerance range. The series includes 37 breakdown voltages with nominal working voltages from 2.4 V to 75 V.

1.2 Features and benefits

- Total power dissipation: ≤ 300 mW
- Two tolerance series: ±2 % and approximately ±5 %
- AEC-Q101 qualified

1.3 Applications

General regulation functions

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _F	forward voltage	I _F = 10 mA [1]	-	-	0.9	V
P _{tot}	total power dissipation	$T_{amb} \le 25 \ ^{\circ}C$ [2]	-	-	300	mW

[1] Pulse test: $t_p \le 100 \ \mu s$; $\delta \le 0.02$

[2] Device mounted on a FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

Working voltage range: nominal 2.4 V to 75 V (E24 range)

Non-repetitive peak reverse power dissipation: ≤ 40 W

nexperia

2. Pinning information

Table 2.	Pinning			
Pin	Symbol	Description	Simplified outline	Graphic symbol
1	К	cathode [1]		
2	A	anode		1 2 006aaa152

[1] The marking bar indicates the cathode.

3. Ordering information

Table 3.Ordering information

Type number	Package	ackage					
	Name	Description	Version				
BZX384 series ^[1]	SC-76	plastic surface-mounted package; 2 leads	SOD323				

[1] The series includes 37 breakdown voltages with nominal working voltages from 2.4 V to 75 V and ± 2 % and ± 5 % tolerances.

4. Marking

Table 4. Marking codes

Type number	Marking code						
BZX384-B2V4	K1	BZX384-B15	M2	BZX384-C2V4	Т3	BZX384-C15	DD
BZX384-B2V7	K2	BZX384-B16	M3	BZX384-C2V7	T4	BZX384-C16	DE
BZX384-B3V0	K3	BZX384-B18	M4	BZX384-C3V0	T5	BZX384-C18	DF
BZX384-B3V3	K4	BZX384-B20	M5	BZX384-C3V3	Т6	BZX384-C20	DG
BZX384-B3V6	K5	BZX384-B22	M6	BZX384-C3V6	T7	BZX384-C22	DH
BZX384-B3V9	K6	BZX384-B24	M7	BZX384-C3V9	Т8	BZX384-C24	DJ
BZX384-B4V3	K7	BZX384-B27	M8	BZX384-C4V3	Т9	BZX384-C27	DK
BZX384-B4V7	K8	BZX384-B30	M9	BZX384-C4V7	Т0	BZX384-C30	DL
BZX384-B5V1	K9	BZX384-B33	N0	BZX384-C5V1	D5	BZX384-C33	DM
BZX384-B5V6	L1	BZX384-B36	N1	BZX384-C5V6	D6	BZX384-C36	DN
BZX384-B6V2	L2	BZX384-B39	N2	BZX384-C6V2	T1	BZX384-C39	DP
BZX384-B6V8	L3	BZX384-B43	N3	BZX384-C6V8	D7	BZX384-C43	DR
BZX384-B7V5	L4	BZX384-B47	N4	BZX384-C7V5	D8	BZX384-C47	DS
BZX384-B8V2	L5	BZX384-B51	N5	BZX384-C8V2	D9	BZX384-C51	DT
BZX384-B9V1	L6	BZX384-B56	N6	BZX384-C9V1	D0	BZX384-C56	DU
BZX384-B10	L7	BZX384-B62	N7	BZX384-C10	T2	BZX384-C62	DV
BZX384-B11	L8	BZX384-B68	N8	BZX384-C11	DA	BZX384-C68	DW
BZX384-B12	L9	BZX384-B75	N9	BZX384-C12	DB	BZX384-C75	DX
BZX384-B13	M1	-	-	BZX384-C13	DC	-	-

BZX384_SERIES
Product data sheet

5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
I _F	forward current		-	250	mA
I _{ZSM}	non-repetitive peak reverse current	[1]	-	see <u>Table 8</u> and <u>9</u>	
P _{ZSM}	non-repetitive peak reverse power dissipation	[1]	-	40	W
P _{tot}	total power dissipation	$T_{amb} \le 25 \ ^{\circ}C$ [2]	-	300	mW
Tj	junction temperature		-65	+150	°C
T _{amb}	ambient temperature		-65	+150	°C
T _{stg}	storage temperature		-65	+150	°C

[1] $t_p = 100 \ \mu s$; square wave; $T_i = 25 \ ^{\circ}C$ before surge

[2] Device mounted on a FR4 PCB, single-sided copper, tin-plated and standard footprint.

6. Thermal characteristics

Table 6. Thermal characteristics							
Symbol	Parameter	Conditions		Min	Тур	Max	Unit
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	<u>[1]</u>	-	-	415	K/W
R _{th(j-sp)}	thermal resistance from junction to solder point		[2]	-	-	110	K/W

[1] Device mounted on a FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Soldering point of cathode tab.

7. Characteristics

Table 7.Characteristics

 $T_j = 25 \ ^{\circ}C$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _F	forward voltage	I _F = 10 mA [1]	-	-	0.9	V
		I _F = 100 mA [1]	-	-	1.1	V

[1] Pulse test: $t_p \le 100 \ \mu s; \ \delta \le 0.02$

Nexperia

BZX384 series

Voltage regulator diodes

Iz = 5 mA Iz = 1 mA Iz = 5 mA	
Min Max Typ Max Typ Max Max Max V _R (V) Min Typ Max Max Max 2V4 B 2.35 2.45 275 600 70 100 500 1 -3.5 -1.6 0 450 6.0	
2V4 B 2.35 2.45 275 600 70 100 50 1 -3.5 -1.6 0 450 6.0	
C 2.2 2.6	
2V7 B 2.65 2.75 300 600 75 100 20 1 -3.5 -2.0 0 450 6.0	
C 2.5 2.9	
3V0 B 2.94 3.06 325 600 80 95 10 1 -3.5 -2.1 0 450 6.0	
C 2.8 3.2	
3V3 B 3.23 3.37 350 600 85 95 5 1 -3.5 -2.4 0 450 6.0	
C 3.1 3.5	
3V6 B 3.53 3.67 375 600 85 90 5 1 -3.5 -2.4 0 450 6.0	6.0
C 3.4 3.8	
3V9 B 3.82 3.98 400 600 85 90 3 1 -3.5 -2.5 0 450 6.0	
C 3.7 4.1	
4V3 <u>B</u> 4.21 4.39 410 600 80 90 3 1 -3.5 -2.5 0 450 6.0	6.0
C 4.0 4.6	
4V7 B 4.61 4.79 425 500 50 80 3 2 -3.5 -1.4 0.2 300 6.0	6.0 6.0
C 4.4 5.0	
5V1 B 5.0 5.2 400 480 40 60 2 2 -2.7 -0.8 1.2 300 6.0	
C 4.8 5.4	
5V6 B 5.49 5.71 80 400 15 40 1 2 -2.0 1.2 2.5 300 6.0	
C 5.2 6.0	
6V2 <u>B</u> 6.08 6.32 40 150 6 10 3 4 0.4 2.3 3.7 200 6.0	
C 5.8 6.6	
6V8 <u>B</u> 6.66 6.94 30 80 6 15 2 4 1.2 3.0 4.5 200 6.0	
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	
0/1 B 802 028 40 100 6 15 05 6 38 55 70 150 30	
10 B 98 102 50 150 8 20 02 7 45 64 80 90 30	
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	
11 B 10.8 11.2 50 150 10 20 0.1 8 54 74 90 85 25	2.5
12 B 11.8 12.2 50 150 10 25 0.1 8 60 84 10.0 85 25	
C 11.4 12.7	

Table 8.Characteristics per type; BZX384-B2V4 to BZX384-C24 $T_i = 25 \ \mathcal{C}$ unless otherwise specified.

BZX384_SERIES
Product data sheet

Nexperia

BZX384 series

Voltage regulator diodes



Nexperia

BZX384 series

Voltage regulator diodes



8. Test information

8.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101* - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

9. Package outline



BZX384 series

Voltage regulator diodes

10. Soldering





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