Centro Astronómico de Yebes

CAY

CRYOGENIC AMPLIFIER REPORT

Cryogenic LNAs for the RAEGE X-Band receiver:

YXA 1181, YXA 1182, YXA 1183

Version 2

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AMPLIFIERS CHANGES RECORD

Amplifiers YXA 1181, 1182 and 1183 were originally used as front-end LNAs in the 8-9 GHz band of a RAEGE tri-band receiver located at Yebes Observatory. Version 1 of this report includes the measurements corresponding to that stage of the three amplifiers. Yebes tri-band receiver was substituted by a wide- band (2-14 GHz) one in 2016 and sent in 2017 to Ny-Alesund (Norway) as a result of an agreement with the Norwegian Mapping Authority (Kartverket) by which technicians of Yebes Observatory would be in charge of the commissioning of the twin telescopes located there.

During the commissioning of the first antenna, several X band amplifiers were damaged in two different episodes. In all cases, the InP transistor of the first stage was destroyed. The most probable cause for the incident was the RF power at X band coming from a ship radar passing nearby at which the antenna was accidentally pointing. A new protocol was fixed in the antenna control software to avoid the azimuths corresponding to the direction of the sea at low elevations.

The amplifiers were repaired mounting new transistors in the first stage, tuned to optimize the performance and measured at cryogenic temperature. To further prevent similar accidents, it was decided to use GaAs devices. These devices withstand higher input power levels without damage. However, the noise performance is around 60% poorer (5.3-5.5 K to 8.6-8.9 K). Taking into account the other noise contributions of the tri-band receiver, the overall noise temperature is degraded from 23 to 28 K. Version 2 of this report reflects the results obtained with these transistors.

YXA 1 4-12 GHz AMPLIFIER REPORT

1. Introduction

YXA series 1 are C+X band low noise cryogenic amplifiers designed and built at the *Centro Astronómico de Yebes* and originally developed for ALMA project. This document includes a description of the amplifiers and how to operate them, details about the tests performed, the measurements techniques utilized and plots with the relevant data collected (an index is provided thereafter). Attached to the document in its digital version will be a collection of files with the numerical data corresponding to the measurements.

The amplifier is intended to be used together with a **cryogenic isolator** connected to its input. PAMTECH has designed several 4-12 GHz models for this purpose like the CWJ1015K9.

The unit should be biased by a **servo controlled power supply**, which sets the gate voltage for any given drain current. Details about a NRAO style power supply produced in Yebes for our HEMT amplifiers are given in the "HEMT bias card report" section.

2. Description and operating conditions of the amplifier

- Figure 1 shows an outside view of the amplifier. RF input and output connectors are SMA. DC connector is a 9 pin microminiature D-type ITT-Cannon. The pinout is provided in figure 2. As seen in the figure, the RF input connector is the one located closer to the DC connector; the serial number of the unit is stamped on the long side of the amplifier, besides de DC connector. All the holes used to fix the lid are M2 thru-holes and can be used from the other side to attach the amplifier to a cold plate. Be aware of the limited length of thread available, due to the small height of the amplifier.

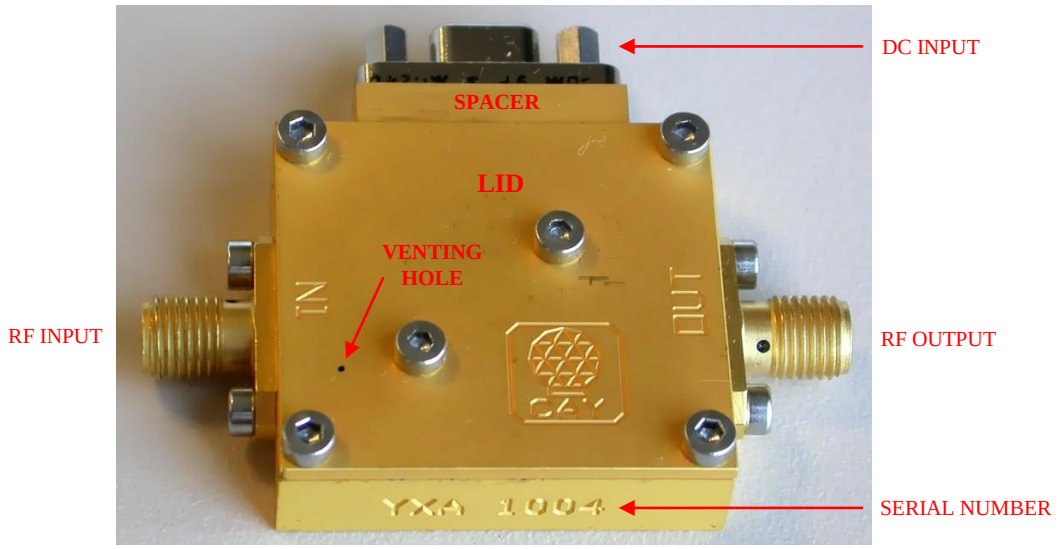

Figure 1: *Amplifier external view. Box dimensions are 32×29×9 mm (excluding connectors and screws).*

- The external dimensions and mechanical interfaces of the amplifier are shown in figure 4.
- These YXA 1 delivered are three stage amplifiers implementing HRL [1] InP transistors. The InP devices are very **ESD sensitive**; cautions must be taken in its manipulation. The bias circuits built in the amplifier include a 10 nF capacitor which acts as a charge divider to prevent damage to the transistors, but no diodes. A ~1:10 voltage divider is also implemented at the gates input lines to improve EMC and protect against ESD: high operating values of the gate voltages are normal. A schematic of these circuits is shown in figure 3. Information on ESD prevention procedures, and safe unit handling and storage is provided in the "ESD and power supply leakage protection of InP HEMT cryogenic amplifiers" section.
- One bias condition has been selected for the amplifier, which optimizes the device for noise, gain ripple, output reflection and gain fluctuations, *keeping the power dissipation below **9 mW***. Some improvement in noise and gain may be expected using a higher bias. Never exceed a drain voltage/current of 1.5 V / 10 mA for InP transistors.

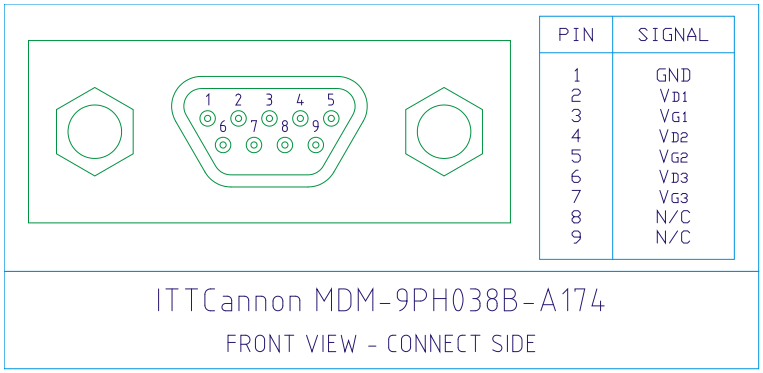

Figure 2: *DC Connector pinout*

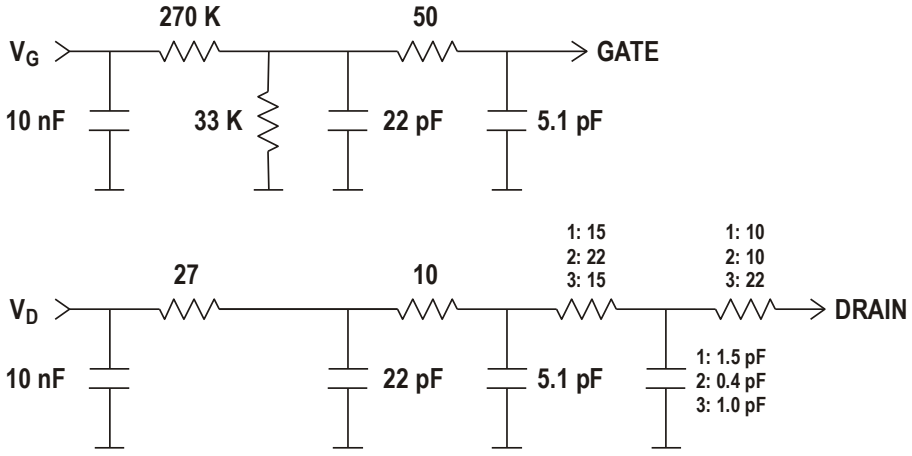

Figure 3: *Schematic of the bias circuits. Gate lines are identical for all stages, while drain lines differ in the component values of the higher frequency filtering and resistive loading sections (they are marked 1:, 2: and 3: after each stage number))*

[1] Transistors provided by Hughes Research Laboratories.

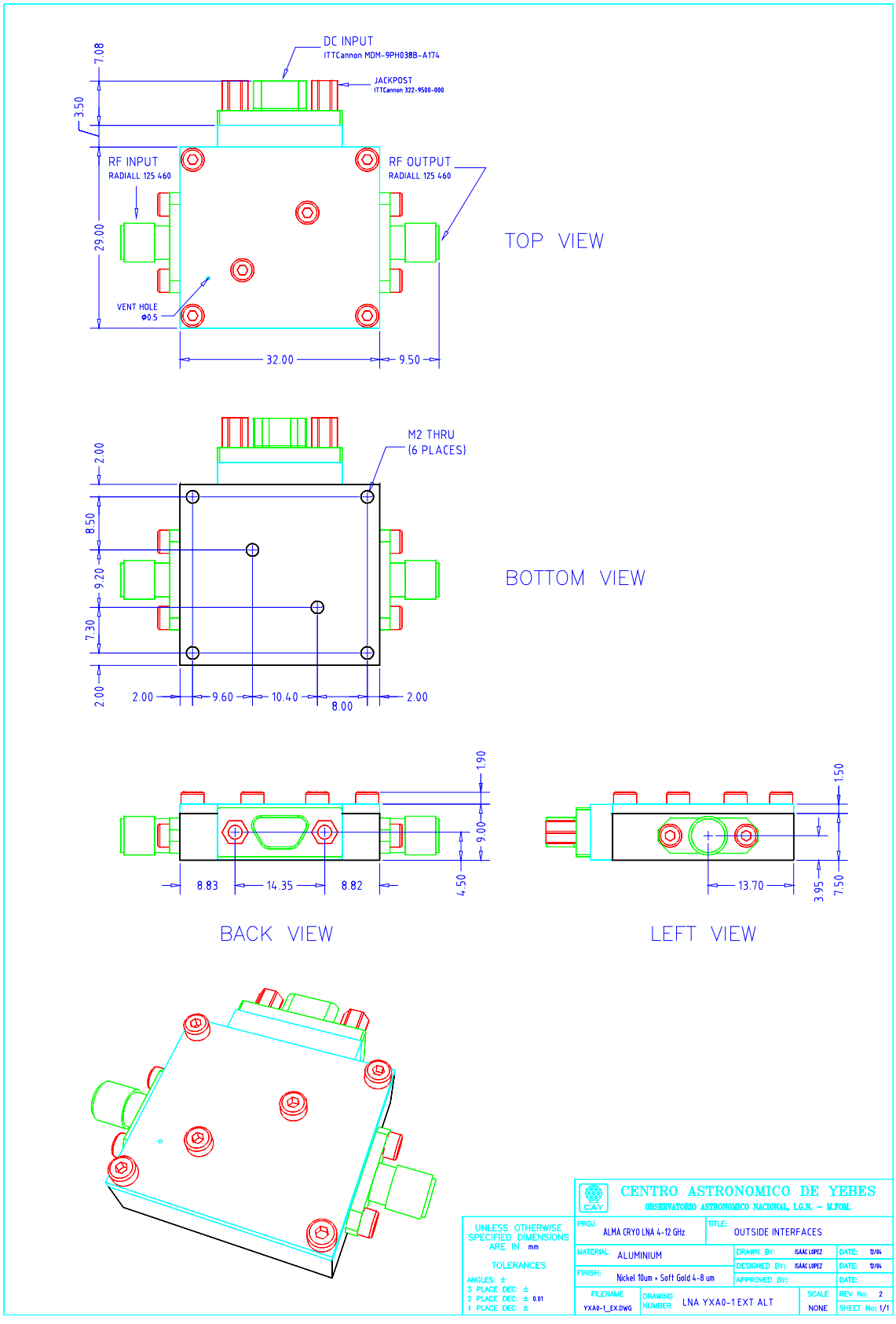

Figure 4: *YXA 1 external dimensions*

3. Measurements

3.1 Description

Noise temperature (and gain) was measured with a system based in a computer controlled Agilent N8975A Noise Figure Meter described in detail in [1], [2]. Room temperature data was obtained with an Agilent N4000A noise diode. The DUT is cooled in a dewar with a CTI 1020 refrigerator. Cryogenic measurements were taken with the "cold attenuator" method, using an Agilent N4002A noise diode (at room temperature) plus a 15 dB attenuator and a Heat-Block device cooled at cryogenic temperature. Temperature is carefully monitored in the attenuator body using a Lake Shore sensor diode. The accuracy of the system for the amplifiers measured can be estimated with methods presented in [3]. For present case, absolute accuracy (@ 2 σ) of measured noise temperature is estimated in 14 K at T_{amb}=297 K and 1.7 K at T_{amb}=14 K. Repeatability is better than this values by an order of magnitude.

S parameters were measured in the same dewar with an Agilent E8364B Vector Network Analyzer from 0.1 to 20 GHz. A detailed description of the measurement procedure used at cryogenic temperature can be found in [1], [2]. The amplifier output is connected to one of the stainless steel dewar transitions and its input to the other through a semi-flexible Cu cable. A full two port calibration is done at room temperature with the electronic calibration kit Agilent N4693-60001 inside the dewar in place of the amplifier, with the same semi-flexible cable. The stainless steel lines are supposed to be invariant with temperature. The Cu cable is measured at cryogenic temperature independently and its loss is taken into account to correct S11 and S21. Time domain gating is used to correct for the residual phase changes in the lines Note that the amplifier design is not optimized for input reflection, as it is intended to be used with an isolator at the input.

Simultaneously, the amplifier was checked for signs of possible out of band instability. Rollet constant was greater than 1 at all frequencies. Selected amplifiers were also tested with a spectrum analyzer Agilent 9565 EC (0-50 GHz) and wide band detector from a HP 8757 A Scalar Network Analyzer in AC (modulated) mode, sensitive to higher frequency oscillations. Stability tests were carried out with a wide range of bias settings.

3.2 Index of plots

We provide plots of the vector network analyzer measurements and noise figure meter measurements at ambient and cryogenic temperatures, for the optimum bias points. A picture of each amplifier is provided for reference purposes.

1. Summary of performance, characteristics and bias
2. Amplifier reference picture
3. Noise and gain measurements
    a. Noise temperature & gain at room temperature
    b. Noise temperature & gain at cryogenic temperature
4. Return loss measurements
    a. Input & output reflection loss at room temperature
    b. Input & output reflection loss at cryogenic temperature

References

[1] J. D. Gallego, I. López-Fernández, C. Diez, "*A Measurement Test Set for ALMA Band 9 Amplifiers*", 1st Radionet Engineering Forum Workshop, 23-24/06/2009, Gothenburg (available at http://www.radionet-eu.org/fp7wiki/lib/exe/fetch.php?media=na:engineering:ew:lopez-fernandez_final.pdf)

[2] I. López-Fernández, J. D. Gallego, C. Diez, A. Barcia, "*Development of Cryogenic IF Low Noise 4-12 GHz Amplifiers for ALMA Radio Astronomy Receivers*", 2006 IEEE MTT-S Int. Microwave Symp. Dig, pp. 1907-1910, 2006.

[3] J. D. Gallego, J. L. Cano, "*Estimation of Uncertainty in Noise Measurements Using Monte Carlo Analysis*", 1st Radionet Engineering Forum Workshop, 23-24/06/2009, Gothenburg (available at http://www.radionet-eu.org/fp7wiki/lib/exe/fetch.php?media=na:engineering:ew:gallego_final.pdf

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ALMA BAND 9 CRYO-LNA REPORT

DATE: 03/11/17

BAND:	4 - 12	S/N:	**YXA 1181**
TRANSISTOR 1st STAGE:	MGFC T-57		
TRANSISTOR 2nd STAGE:	HRL 150x0.1 um T-69		
TRANSISTOR 3rd STAGE:	HRL 150x0.1 um T-69		

ROOM TEMPERATURE DATA T = 295.2

OPTIMUM BIAS	V_{d1} = 2.5	I_{d1} = 15	V_{g1} = -2.18
	V_{d2} = 1.5	I_{d2} = 10	V_{g2} = -4.07
	V_{d3} = 1.5	I_{d3} = 10	V_{g3} = -3.75

AVERAGE NOISE TEMP:	59.9	MIN. INPUT RETURN LOSS:	-4.2
AVERAGE GAIN:	31.8	MIN. OUTPUT RETURN LOSS:	-10.7

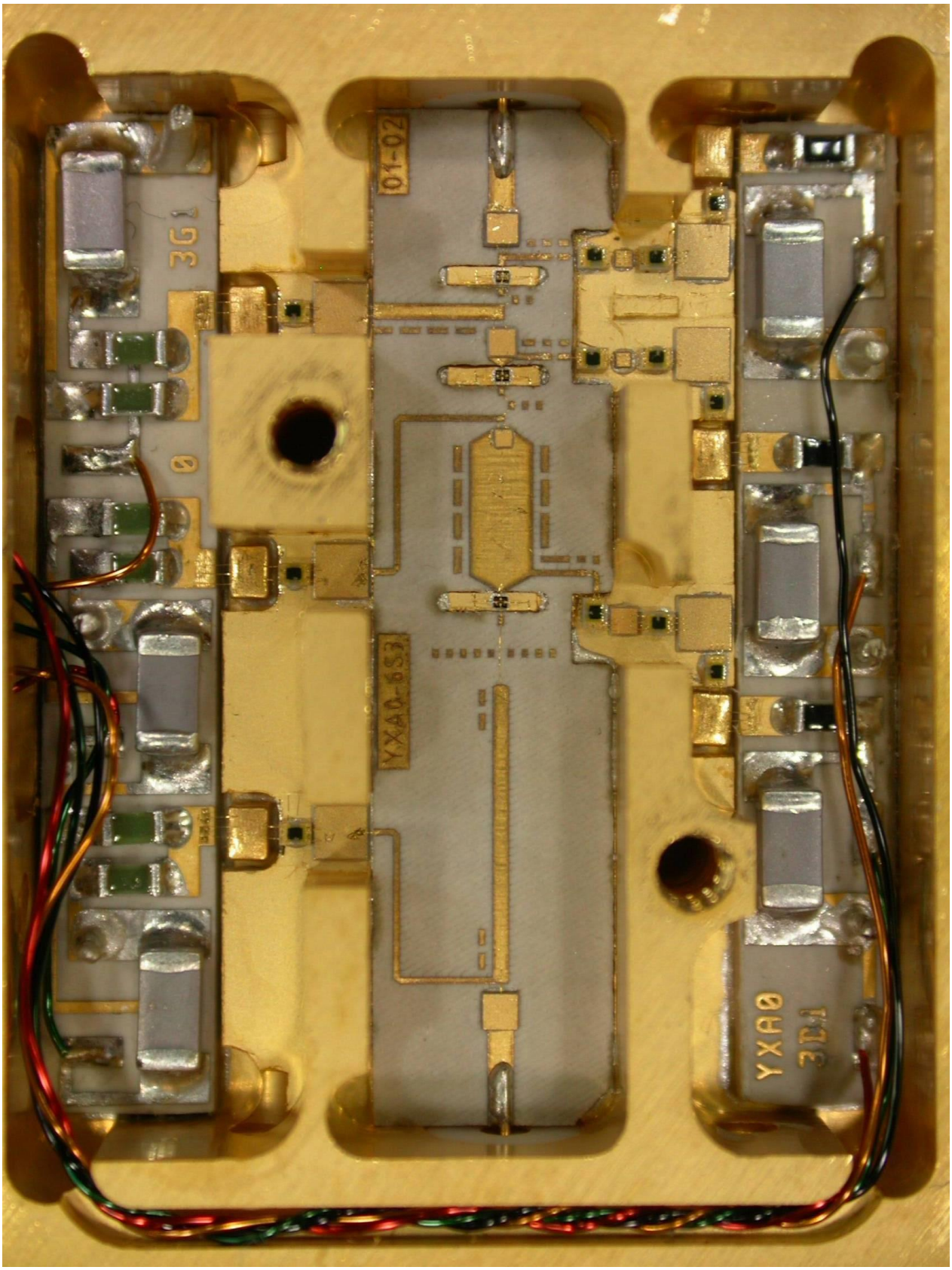
CRYOGENIC TEMPERATURE DATA T = 13.5

OPTIMUM BIAS	V_{d1} = 2.00	I_{d1} = 6.0	V_{g1} = -2.76
	V_{d2} = 0.60	I_{d2} = 4.0	V_{g2} = -1.45
(P_{diss} = 16.80 mW)	V_{d3} = 0.60	I_{d3} = 4.0	V_{g3} = -1.33

AVERAGE NOISE TEMP:	8.75	MAX. / MIN. NOISE TEMP:	9.95	6.97
AVERAGE GAIN:	32.1	GAIN SPAN FULL BAND / 2 GHz:	1.4	1.2
MIN. INPUT RETURN LOSS:	-4.0	MIN. OUTPUT RETURN LOSS:	-12.6	

REMARKS: Gain data from VNA measurements

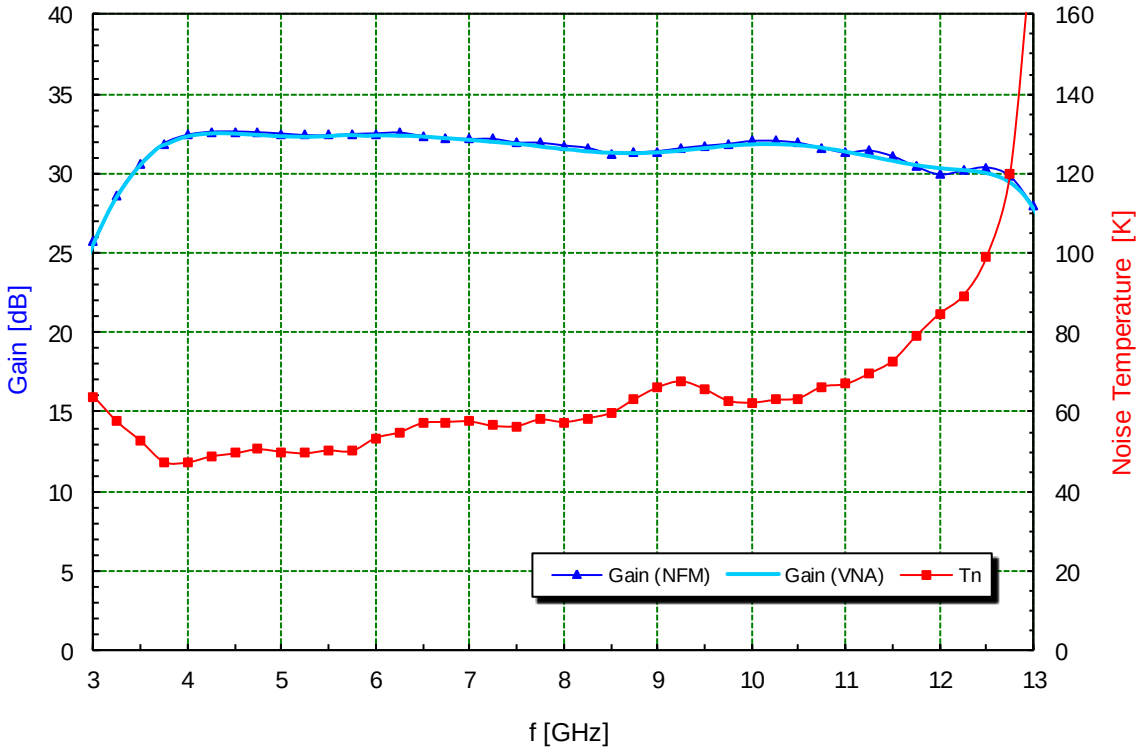
V_d in Volts, I_d in mA, Noise temperature in K, Gain and Return loss in dB, Frequency band in GHz



Reference picture of YXA 1181 (10) inside (bias and microwave cavities)

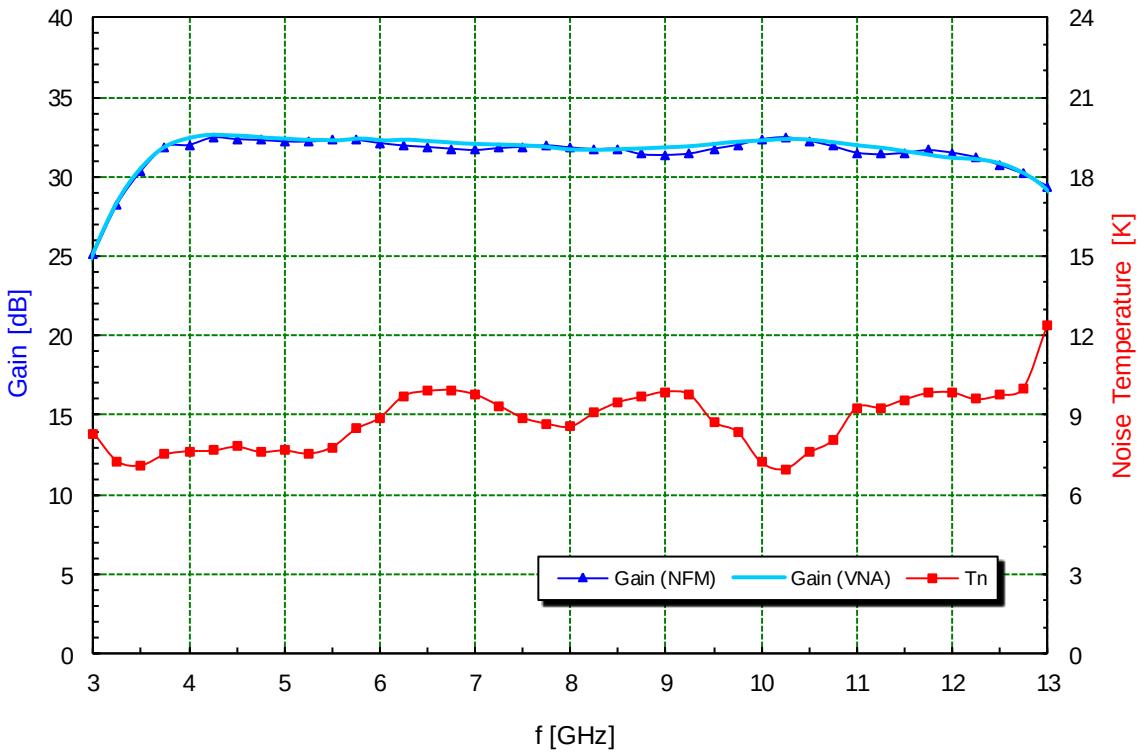
YXA 1181 (10)

$V_{D(1,2,3)}$= (2.5,1.5,1.5) $I_{D(1,2,3)}$= (15,10,10) **T=295.2**



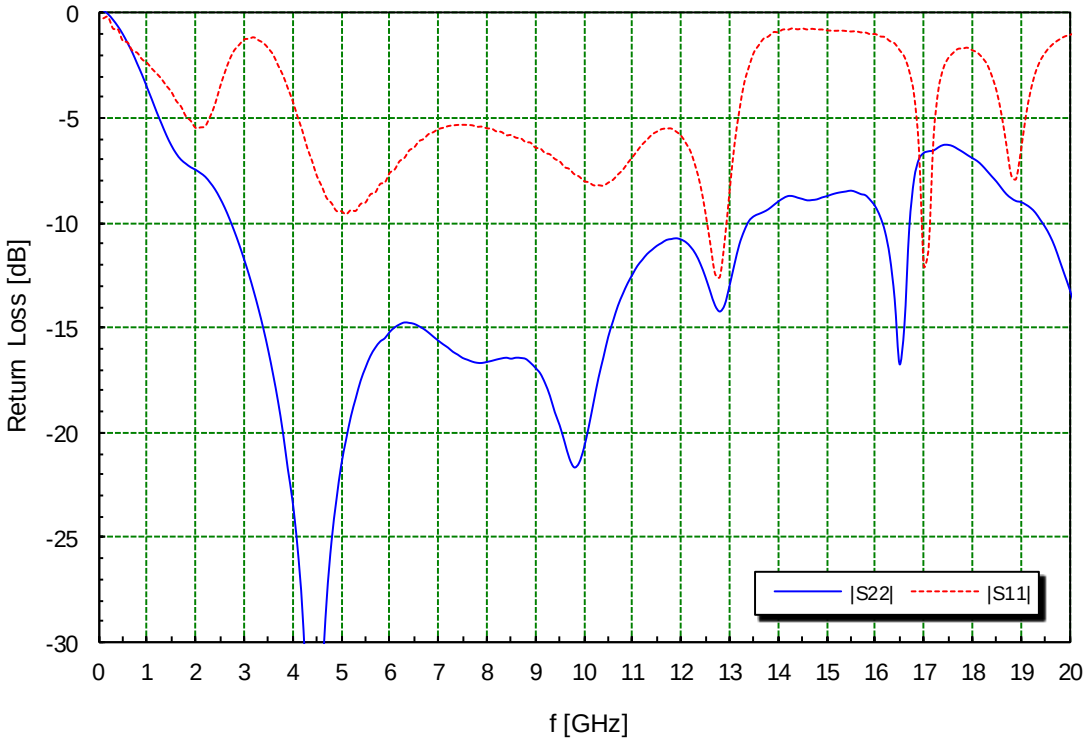
YXA 1181 (10)

$V_{D(1,2,3)}$= (2,0.6,0.6) $I_{D(1,2,3)}$= (6,4,4) **T=13.5**



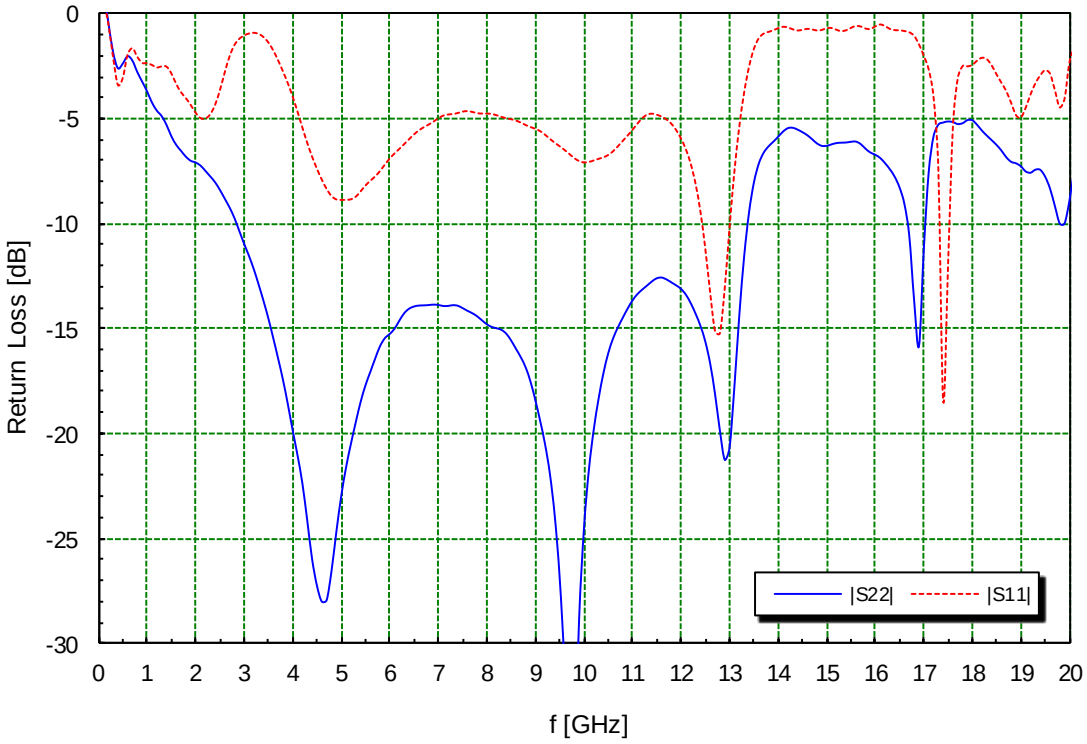
YXA 1181 (10)

VD=(2.5,1.5,1.5) ID=(15,10,10) **T=295.2**



YXA 1181 (10)

VD=(2.0,.6,.6) ID=(6,4,4) **T=20**



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ALMA BAND 9 CRYO-LNA REPORT

DATE: 03/11/17

BAND:	4 - 12	S/N:	**YXA 1182**
TRANSISTOR 1st STAGE:	MGFC 4419G T-57		
TRANSISTOR 2nd STAGE:	HRL 150x0.1 um T-69		
TRANSISTOR 3rd STAGE:	HRL 150x0.1 um T-69		

ROOM TEMPERATURE DATA T = 14.0

OPTIMUM BIAS	V_{d1} = 2.5	I_{d1} = 15	V_{g1} = -2.11
	V_{d2} = 1.5	I_{d2} = 10	V_{g2} = -4.44
	V_{d3} = 1.5	I_{d3} = 10	V_{g3} = -3.96

AVERAGE NOISE TEMP:	60.6	MIN. INPUT RETURN LOSS:	-4.5
AVERAGE GAIN:	31.2	MIN. OUTPUT RETURN LOSS:	-10.6

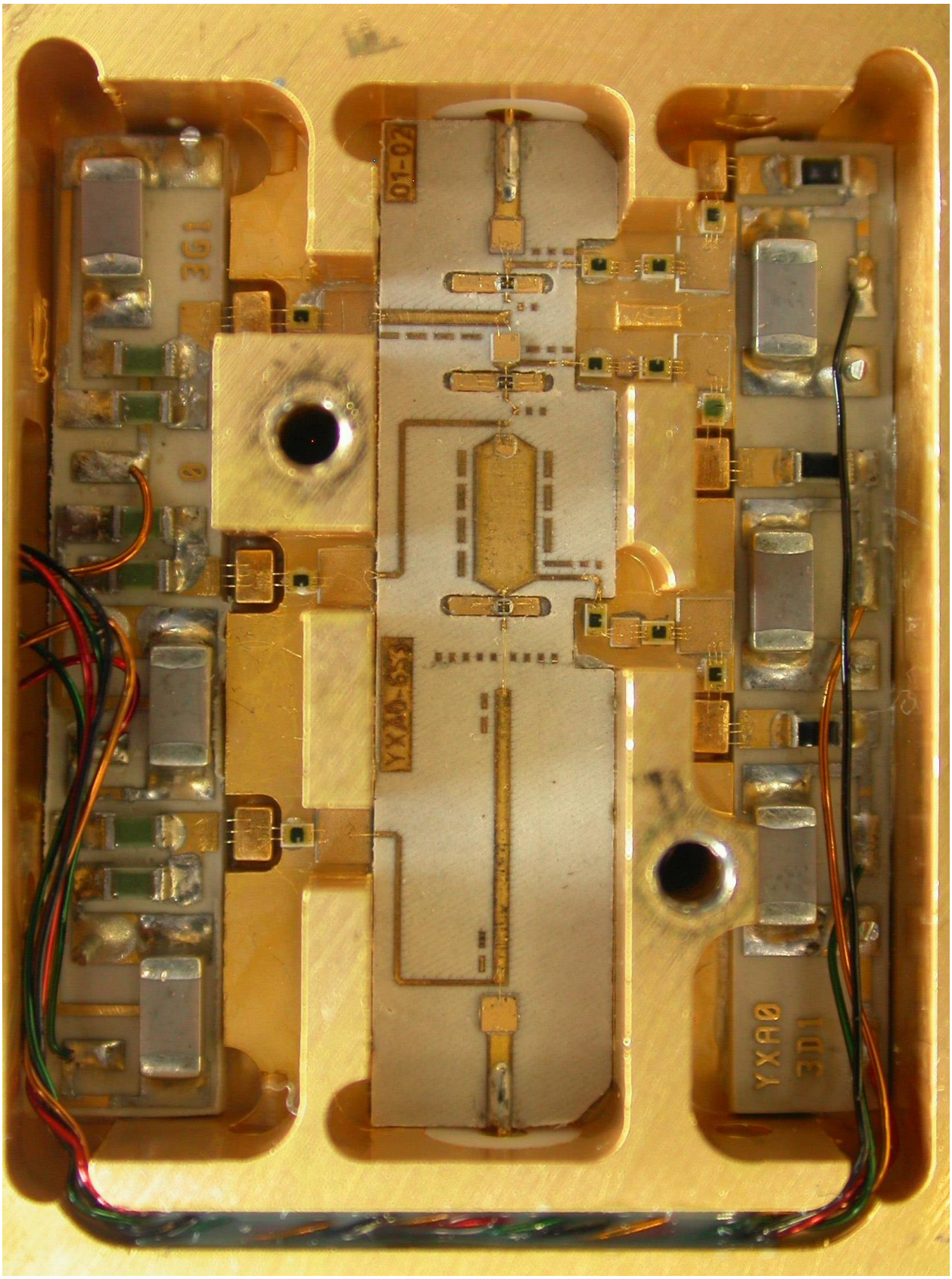
CRYOGENIC TEMPERATURE DATA T = 13.6

OPTIMUM BIAS	V_{d1} = 2.40	I_{d1} = 6.0	V_{g1} = -3.02
	V_{d2} = 0.60	I_{d2} = 4.0	V_{g2} = -1.55
(P_{diss} = 19.20 mW)	V_{d3} = 0.60	I_{d3} = 4.0	V_{g3} = -1.37

AVERAGE NOISE TEMP:	8.58	MAX. / MIN. NOISE TEMP:	10.11	6.66
AVERAGE GAIN:	31.2	GAIN SPAN FULL BAND / 2 GHz:	1.4	1.2
MIN. INPUT RETURN LOSS:	-4.2	MIN. OUTPUT RETURN LOSS:	-13.1	

REMARKS: Gain data from VNA measurements

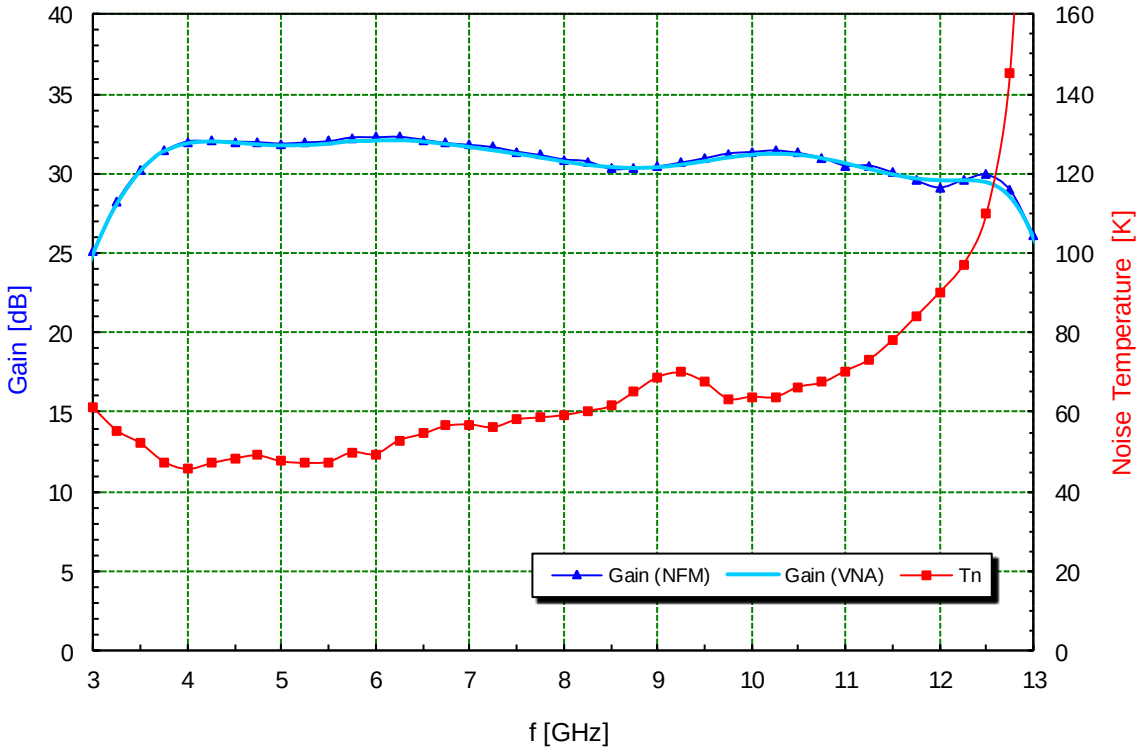
V_d in Volts, I_d in mA, Noise temperature in K, Gain and Return loss in dB, Frequency band in GHz



Reference picture of YXA 1182 (14) inside (bias and microwave cavities)

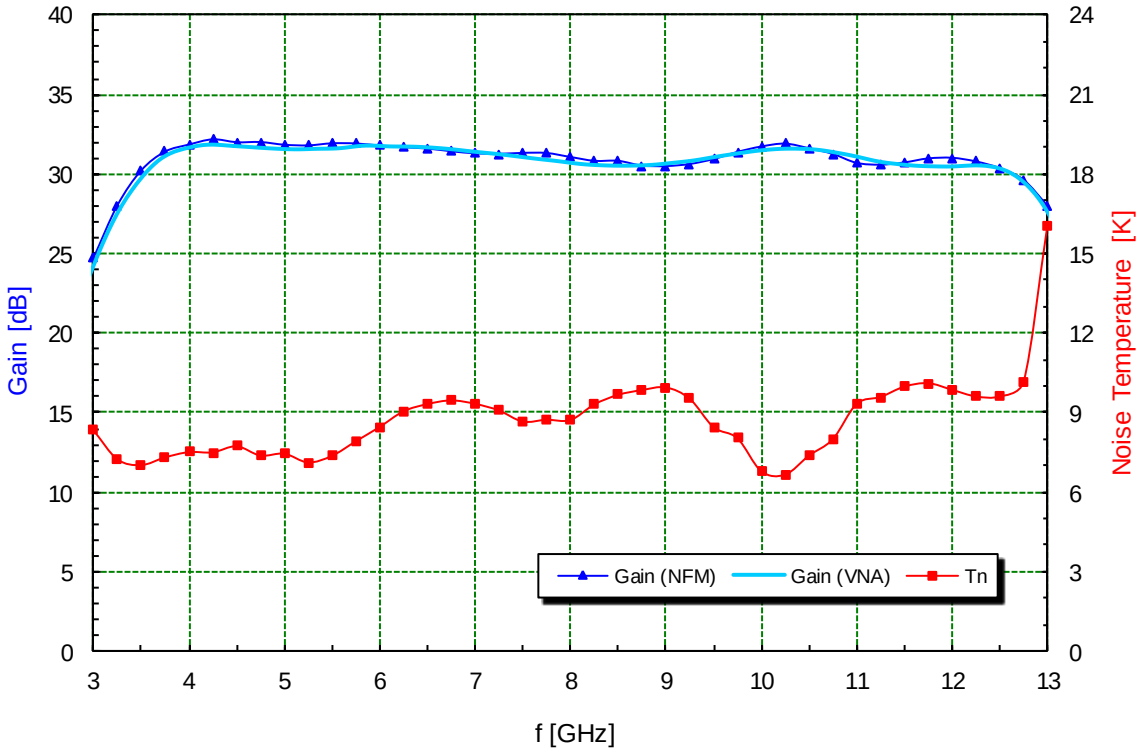
YXA 1182 (14)

$V_{D(1,2,3)}$= (2.5,1.5,1.5) $I_{D(1,2,3)}$= (15,10,10) **T=14**



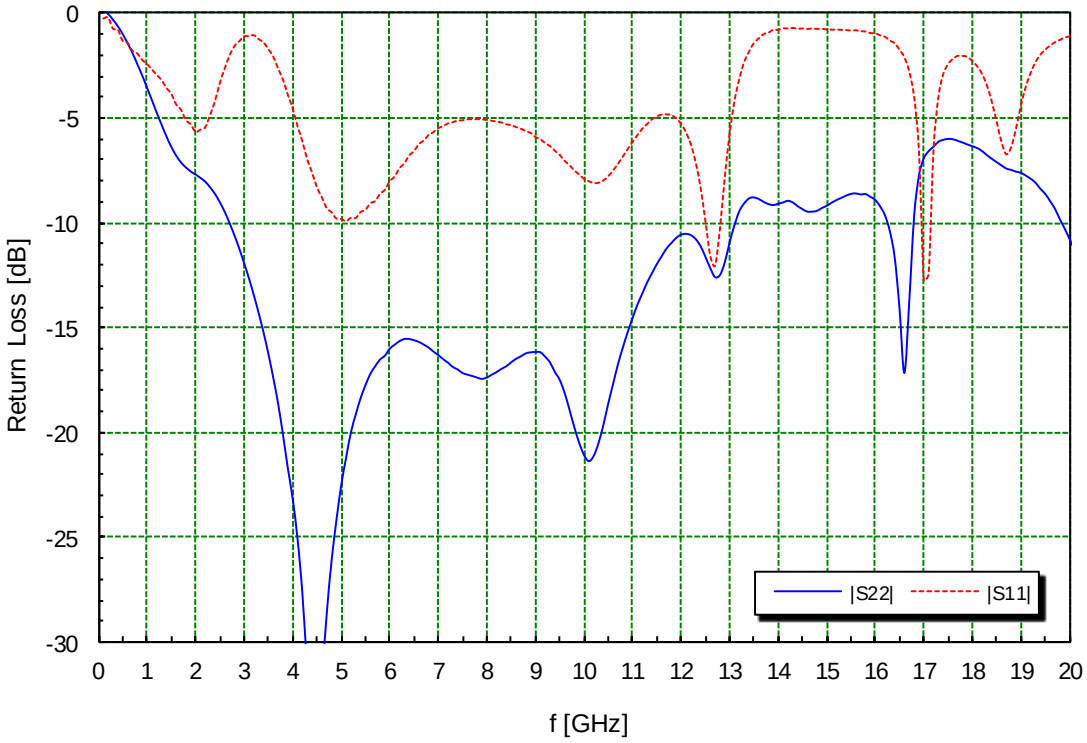
YXA 1182 (14)

$V_{D(1,2,3)}$= (2.4,0.6,0.6) $I_{D(1,2,3)}$= (6,4,4) **T=13.6**



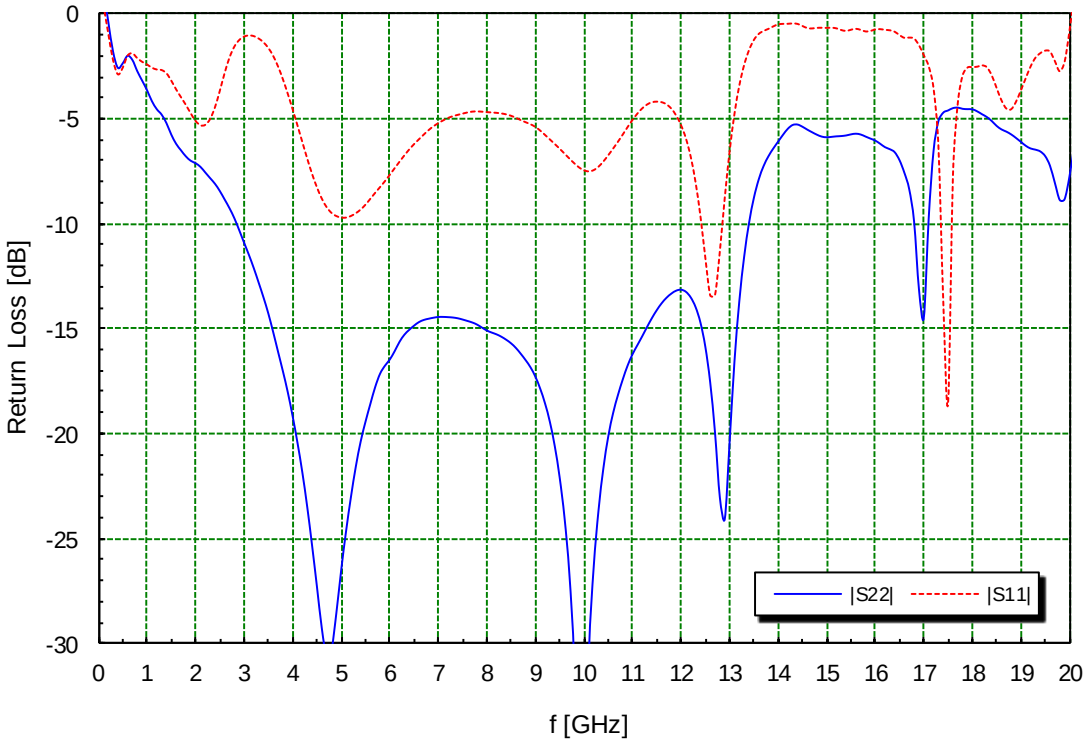
YXA 1182 (14)

VD=(2.5,1.5,1.5) ID=(15,10,10) **T=14**



YXA 1182 (14)

VD=(2.4,.6,.6) ID=(6,4,4) **T=17**



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ALMA BAND 9 CRYO-LNA REPORT

DATE: 03/11/17

BAND:	4 - 12	S/N:	YXA 1183
TRANSISTOR 1st STAGE:	MGFC 4419G T-57		
TRANSISTOR 2nd STAGE:	HRL 150x0.1 um T-69		
TRANSISTOR 3rd STAGE:	HRL 150x0.1 um T-69		

ROOM TEMPERATURE DATA T = 295.3

OPTIMUM BIAS	V_{d1} = 2.5	I_{d1} = 15	V_{g1} = -2.09
	V_{d2} = 1.5	I_{d2} = 10	V_{g2} = -4.27
	V_{d3} = 1.5	I_{d3} = 10	V_{g3} = -4.16

AVERAGE NOISE TEMP:	61.6	MIN. INPUT RETURN LOSS:	-3.9
AVERAGE GAIN:	31.7	MIN. OUTPUT RETURN LOSS:	-12.1

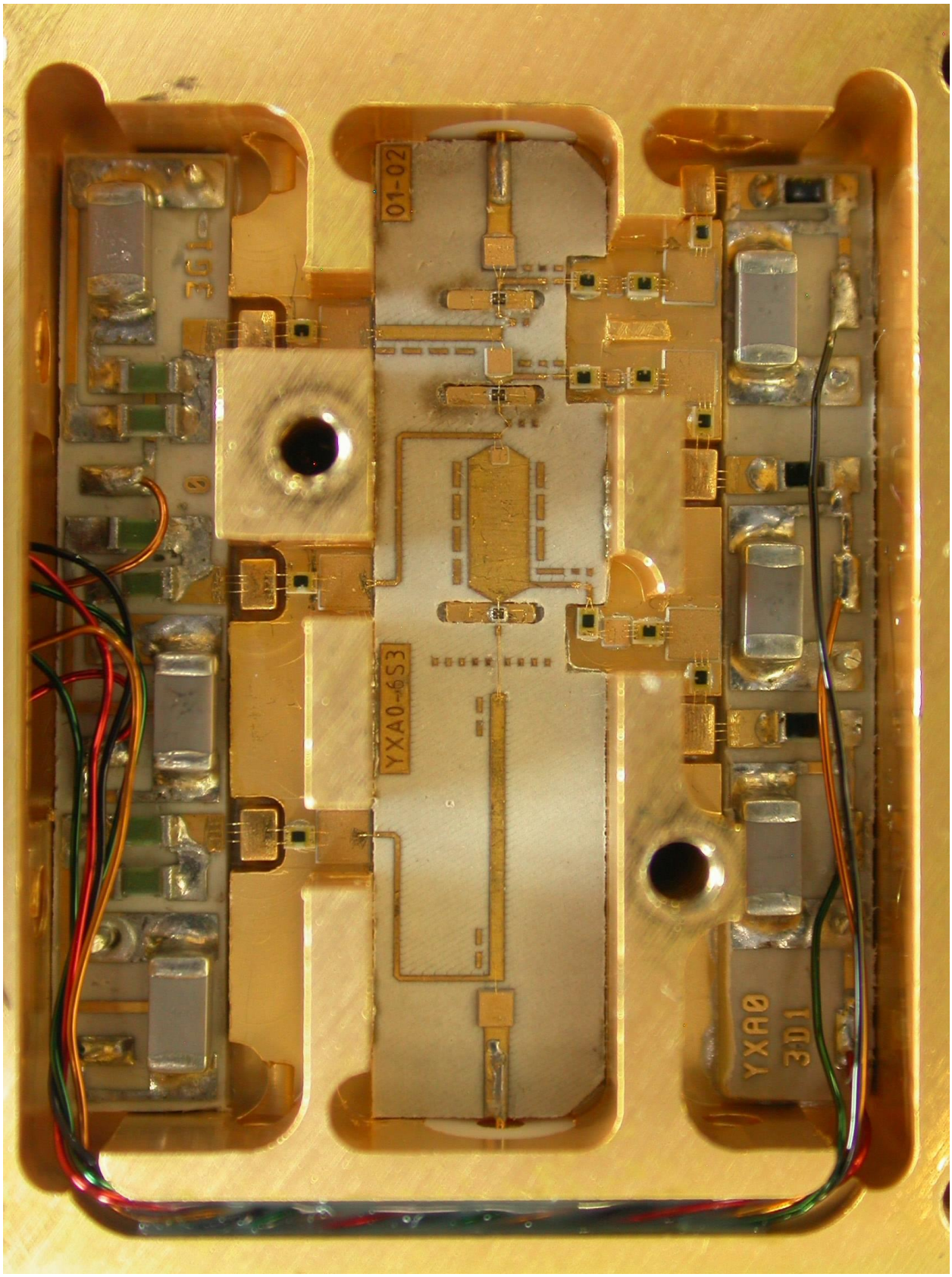
CRYOGENIC TEMPERATURE DATA T = 13.5

OPTIMUM BIAS	V_{d1} = 2.00	I_{d1} = 6.0	V_{g1} = -2.62
	V_{d2} = 0.60	I_{d2} = 4.0	V_{g2} = -1.56
(P_{diss} = 16.80 mW)	V_{d3} = 0.60	I_{d3} = 4.0	V_{g3} = -1.53

AVERAGE NOISE TEMP:	8.92	MAX. / MIN. NOISE TEMP:	10.48	7.14
AVERAGE GAIN:	32.3	GAIN SPAN FULL BAND / 2 GHz:	1.5	1.1
MIN. INPUT RETURN LOSS:	-3.9	MIN. OUTPUT RETURN LOSS:	-12.9	

REMARKS: Gain data from VNA measurements

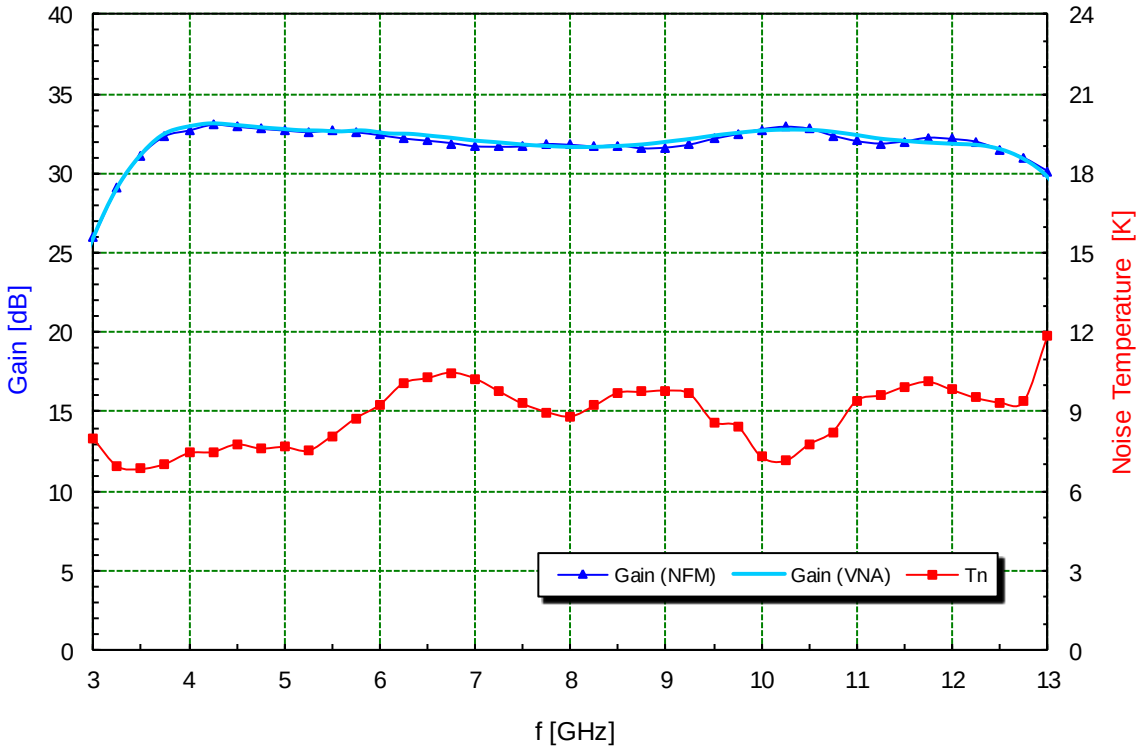
V_d in Volts, I_d in mA, Noise temperature in K, Gain and Return loss in dB, Frequency band in GHz



Reference picture of YXA 1183 (7) inside (bias and microwave cavities)

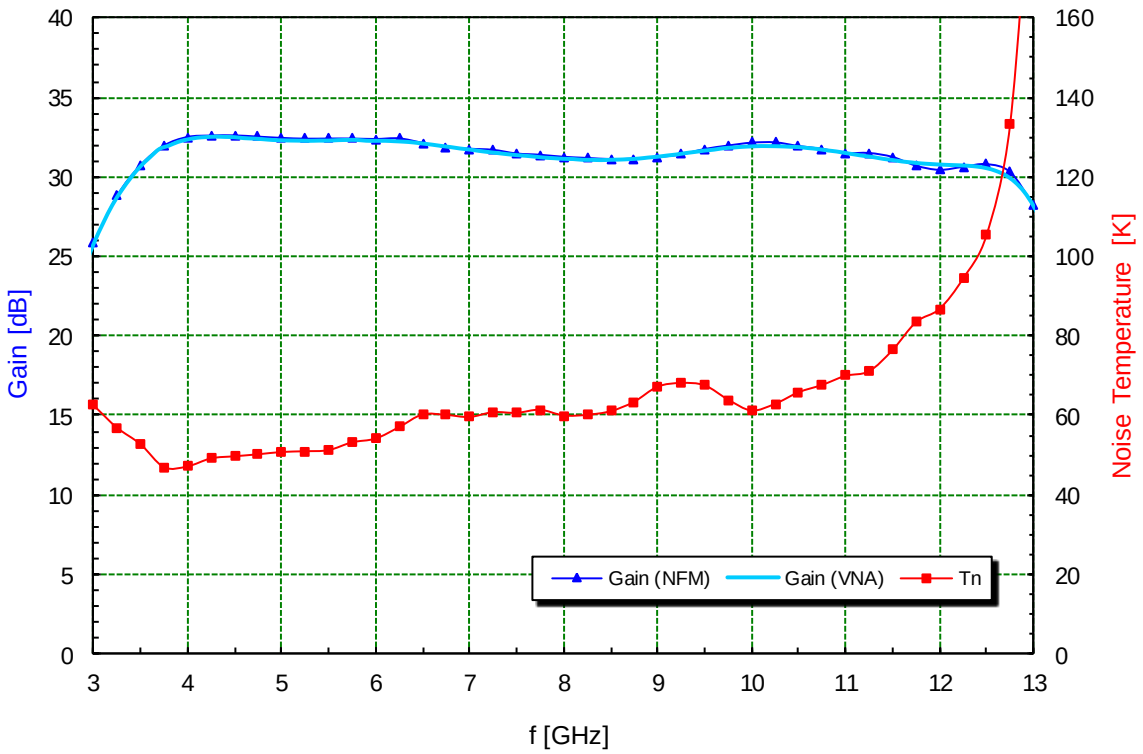
YXA 1183 (7)

$V_{D(1,2,3)}$= (2,0.6,0.6) $I_{D(1,2,3)}$= (6,4,4) **T=13.5**



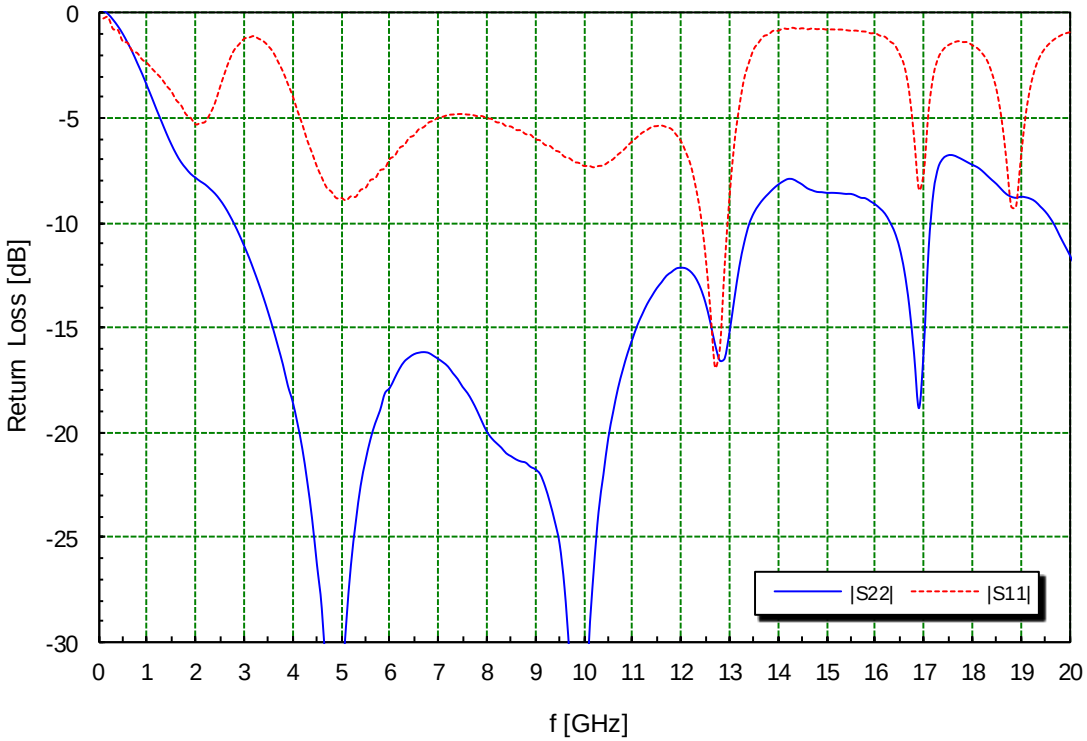
YXA 1183 (7)

$V_{D(1,2,3)}$= (2.5,1.5,1.5) $I_{D(1,2,3)}$= (15,10,10) **T=295.3**



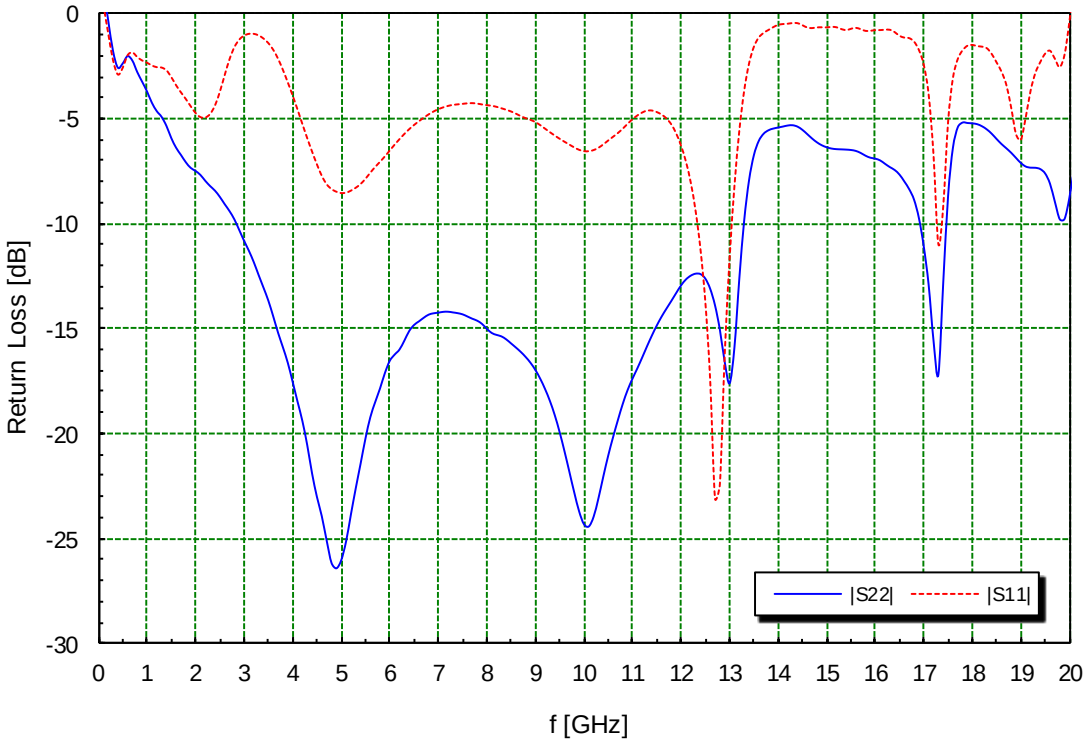
YXA 1183 (7)

VD=(2.5,1.5,1.5) ID=(15,10,10) **T=295.3**



YXA 1183 (7)

VD=(2.0,.6,.6) ID=(6,4,4) **T=20**



HEMT BIAS CARD REPORT

1. Introduction

A power supply card is needed to operate the amplifier. This report provides information about an NRAO-style design for a power supply card manufactured at CAY. The schematic is presented in figure 1. Drawings of the PC board and details of the connectors are presented in the included documentation.

2. Description and operation

The power supply card provides signals to monitor the correct operation of each of the stages of the amplifiers, and to facilitate the adjustment. The parameters available are the drain voltage (V_d), drain current (I_d) and gate voltage (V_g). Note that the monitor signal of the drain current provides a voltage reading proportional to the current (0.1 V per mA, for Id=5 mA the reading is 0.5 Volt). The monitor signals are available in the PCB edge connector pins, and as test points in the front part of the PCB.

The power supply is a feedback system implemented with a quad operational amplifier per each HEMT amplifier stage, and can be easily understood observing the attached schematic for a single stage (figure 1). The desired drain voltage and drain current of the HEMT are selected in variable resistors, and the power supply finds the adequate value of the gate voltage. In these way, any change in the transconductance of the HEMT is compensated by changing the gate voltage, keeping the drain current constant.

3. Index of figures and tables

Addendum: Modifications to the standard design

To allow a sufficient range of gate voltages when using amplifiers with gate voltage dividers, zenner diodes D3, D6, D9 and D12 have been replaced by two zenner diodes of the same type connected in opposition (anti-series).

Important: This changes affect figures 1,2,5 and table 1

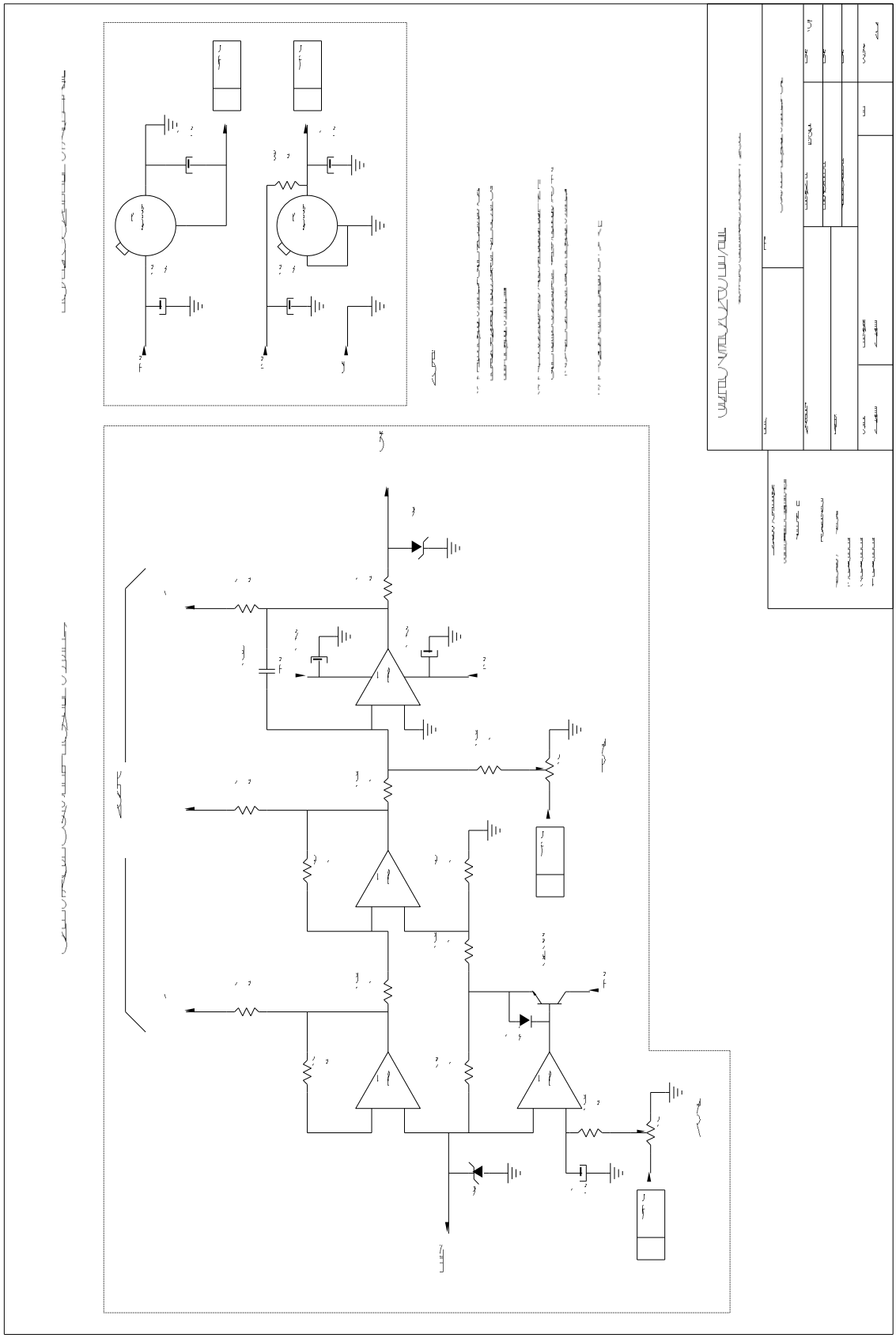


Figure 1: *One stage schematic*

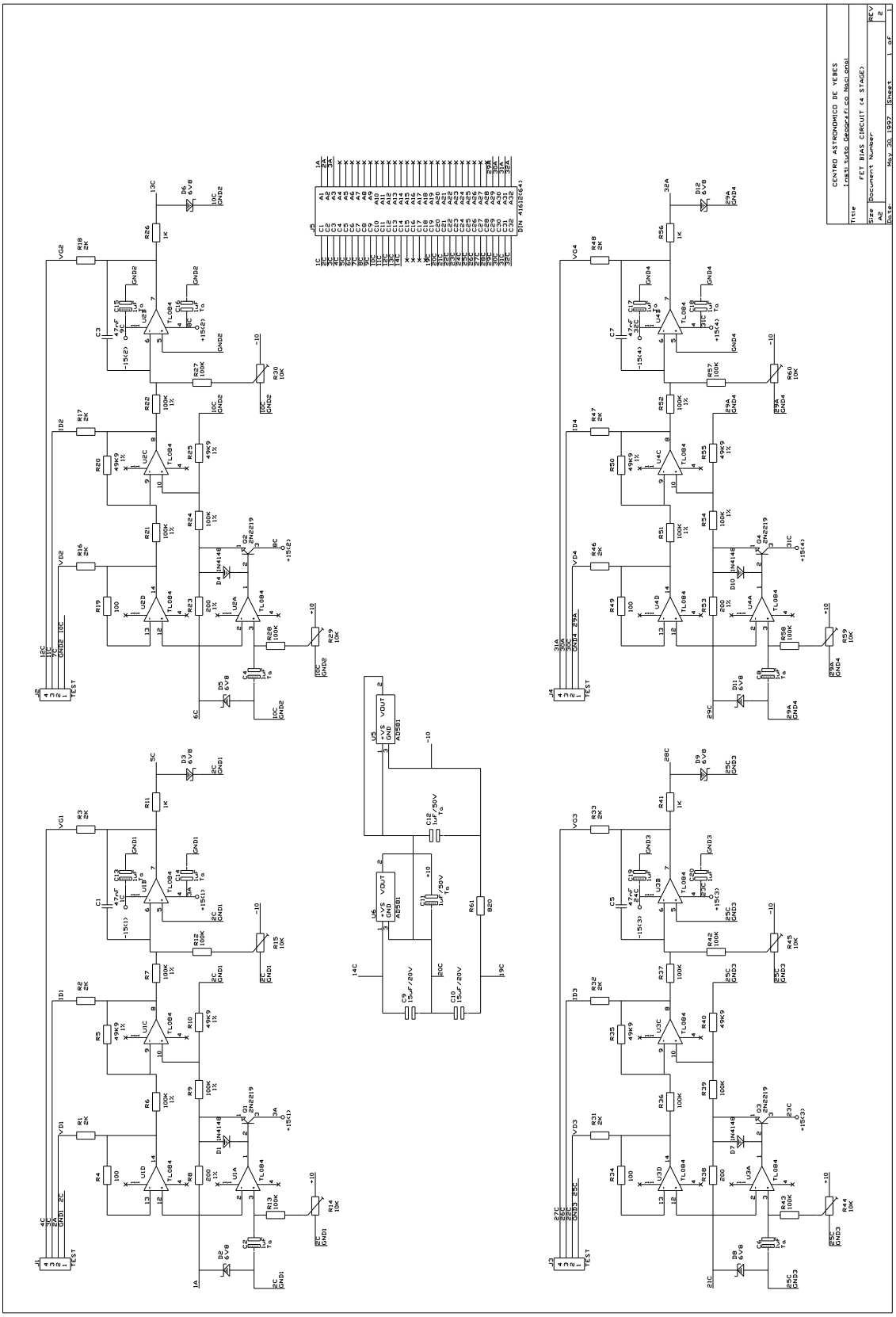


Figure 2: *PC Board schematic*

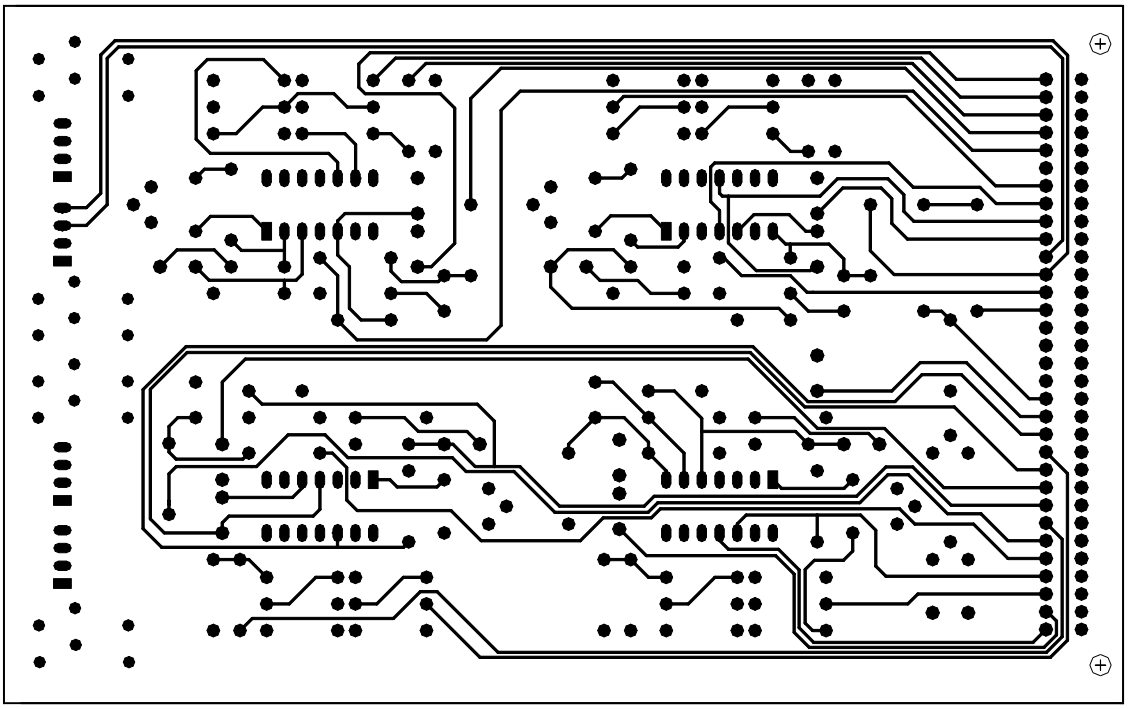


Figure 3: *PC Board tracks - Component side*

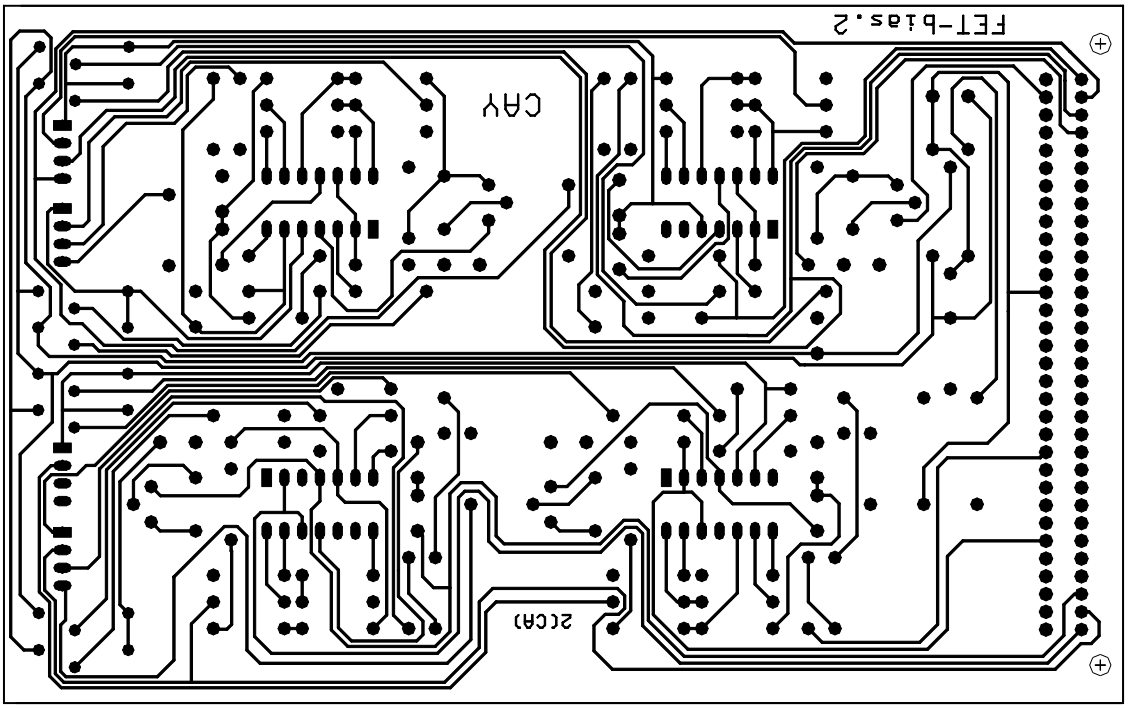


Figure 4: *PC Board tracks – Solder side*

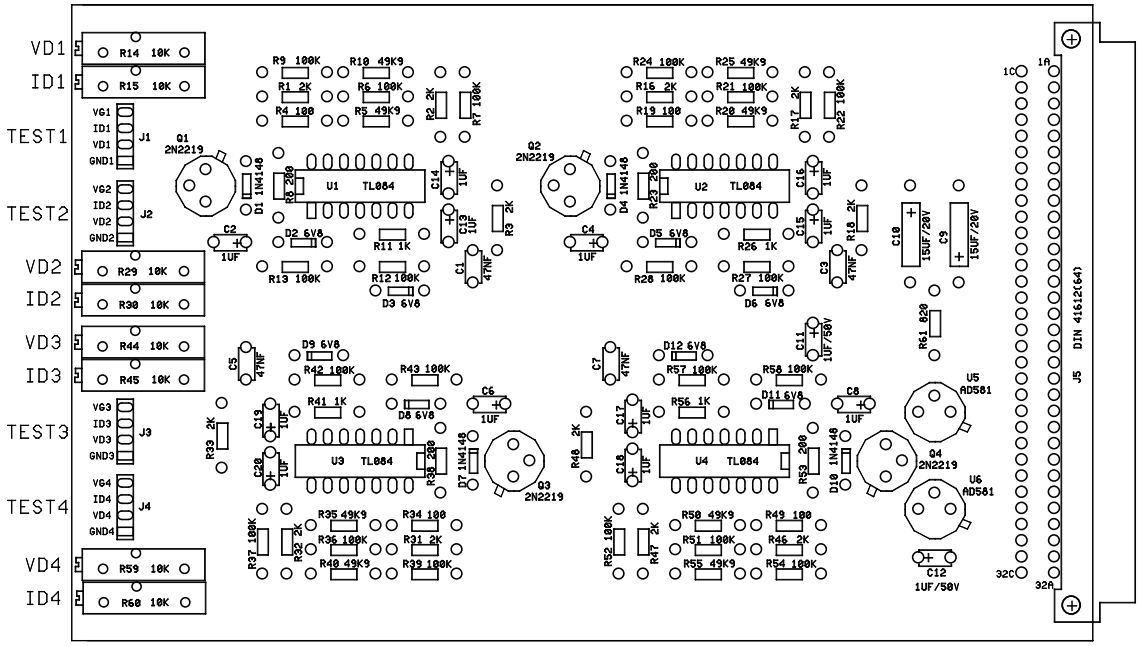


Figure 5: *PC Board components*

Table 1: *Power supply list of components*

FET BIAS CIRCUIT (4 STAGE) **Revised: January 31, 1997**
Revision: 2

Bill Of Materials **March 20, 1997** **Page 1**

Item	Quantity	Reference	Part	DESCRIPTION
1	4	C1,C3,C5,C7	47nF	Polyester, 63V
2	12	C2,C4,C6,C8,C11,C12,C13, C14,C15,C16,C17,C18,C19, C20	1uF	Tantalum, 50V
3	2	C10,C9	15uF/20V	Electrolytic
4	8	D2,D3,D5,D6,D8,D9,D11, D12	6V8	
5	4	D1,D4,D7,D10	1N4148	
6	4	J1,J2,J3,J4	TEST	4pin, SIL BAR
7	1	J5	DIN 41612(64)	
8	4	Q1,Q2,Q3,Q4	2N2219	
9	12	R1,R2,R3,R16,R17,R18,R31, R32,R33,R46,R47,R48	2K	1/4W, 1%
10	4	R4,R19,R34,R49	100	1/4W, 5%
11	8	R5,R10,R20,R25,R35,R40, R50,R55	49K9	1/4W, 1%
12	20	R6,R7,R9,R12,R13,R21,R22, R24,R27,R28,R36,R37,R39, R42,R43,R51,R52,R54,R57, R58	100K	1/4W, 1%
13	4	R8,R23,R38,R53	200	1/4w, 1%
14	4	R11,R26,R41,R56	1K	1/4W, 5%
15	8	R14,R15,R29,R30,R44,R45, R59,R60	10K	20T H POT
16	1	R61	820	1/4W, 5%
17	4	U1,U2,U3,U4	TL084	
18	2	U6,U5	AD581	

Table 2: *PC Board edge connector wiring table*

DIN 41612

PIN NUMBER	DESCRIPTION	PIN NUMBER	DESCRIPTION
1 a	DRAIN 1 (1)	11 c	Id (2)
2 a	Vd 1 (1)	12 c	Vg (2)
3 a	+15 V (1)	13 c	GATE (2)
-	-	14 c	+15 V (to potenc.)
29 a	GND (4)	-	-
30 a	Id (4)	19 c	-15 V (to potenc.)
31 a	Vg (4)	20 c	GND (to potenc.)
32 a	GATE (4)	21 c	DRAIN 3
-	-	22 c	Vd (3)
1 c	-15 V (1)	23 c	+15 V (3)
2 c	GND (1)	24 c	-15 V (3)
3 c	Id (1)	25 c	GND (3)
4 c	Vg (1)	26 c	Id (3)
5 c	GATE (1)	27 c	Vg (3)
6 c	DRAIN (2)	28 c	GATE (3)
7 c	Vd (2)	29 c	DRAIN (4)
8 c	+15 V (2)	30 c	Vd (4)
9 c	-15 V (2)	31 c	+15 V (4)
9 c	-15 V (2)	32 c	-15 V (4)
10 c	GND (2)		

Table 3: *Cable connections for a 3-stage HEMT amplifier*

15 PIN 'D' CONNECTOR (BIAS MONITOR)

PIN NUMBER	DESCRIPTION
1	SIGNAL GROUND
2	Vd 1
3	Id 1
4	Vg 1
5	Vd 2
6	Id 2
7	Vg 2
8	Vd 3
9	Id 3
10	Vg 3
11	N.C.
12	N.C.
13	N.C.
14	N.C.
15	N.C.

9 PIN 'D' CONNECTOR (TO HEMT AMPLIFIER)

PIN NUMBER	DESCRIPTION
1	SIGNAL GROUND
2	DRAIN 1
3	GATE 1
4	DRAIN 2
5	GATE 2
6	DRAIN 3
7	GATE 3
8	N.C.
9	N.C.

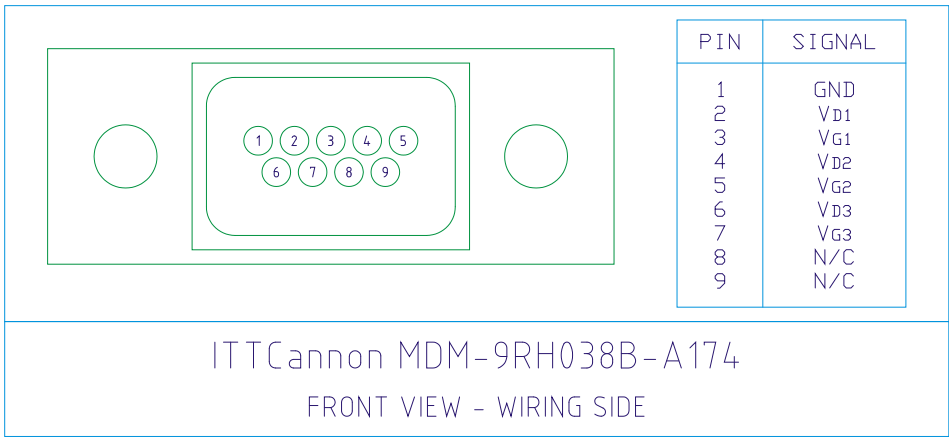


Figure 6: *Microtech connector plug (in cable) for a 3-stage HEMT amplifier*

ESD AND POWER SUPPLY LEAKAGE PROTECTION OF InP CRYOGENIC HEMT AMPLIFIERS

Introduction

Cryogenic amplifiers made with InP HEMTs have been found very sensitive to ESD (electrostatic discharges) and leakage from the power supplies. The handling of these devices requires especial precautions beyond the normal care taken with cryogenic amplifiers made with commercial GaAs HEMTs. Especial procedures should be followed during assembly of the amplifiers as well as during tests and operation to avoid permanent damage to the devices. The most common mode of failure is the total or partial destruction of the gate of the transistors. Partially damaged devices may loose one or more gate fingers and show poor or no pinch off, even if the gate junction still show diode characteristics. Totally damaged devices may appear as a short circuit (or low resistance) from drain to source. Sometimes, but not often, the device may appear as an open circuit.

ESD is not the only problem. Leakage of soldering irons, bonding machines and even power supplies of the amplifiers has produced many failures. All the equipment used in the assembly test and operation of the amplifiers should be checked for leakage. Most of the field problems detected have been caused by 50 Hz current leakage of input transformers of floating DC power supplies. This leakage is due to the capacitive coupling between primary and secondary of the transformers and it is always present unless there is a grounded faraday shield between the two windings or other especial precautions are taken

Procedure for assembly of the amplifiers

1. Technicians manipulating amplifiers should wear grounded wrist straps.
2. The bench for the assembly of the amplifiers should have a dissipative map connected to ground.
3. A short circuit should be put in the power connector of the amplifier at all times during assembly (the short circuit should short all pins together to the case). The short circuit will only be removed for testing the amplifier or when connected for operation.
4. Coaxial SMA short circuits should be connected to input and output RF connectors at all times during assembly. The short circuits will only be removed for testing the amplifier or when connected for operation.
5. The soldering irons used for assembly should be adequately grounded. It should be checked that no voltage respect to ground is measured on the tip with the soldering iron on and off. The maximum voltage allowed will be 0.020 Vrms respect to ground measured with a high input impedance (> 10 MΩ) voltmeter in AC mode.
6. The tip of the bonding and welding machines used for assembly of the amplifier should be adequately grounded. It should be checked that no voltage respect to ground is measured with machines on or off. The maximum voltage allowed will be 0.020 Vrms respect to ground measured with a high input impedance (> 10 MΩ) voltmeter in AC mode.
7. Be very careful with any measurement instrument used during assembly. If ohmmeters are used for verification of internal cabling, battery operated units are preferred. Make all necessary verifications before the assembly of the transistors when possible. The assembly of the transistors should be the last operation to avoid unnecessary risks.

Procedure for test and operation of the amplifiers

1. The amplifier should be kept with a short circuit in the power connector when not in use. The short circuit should short all pins together and to the case. The short circuit should only be removed if adequate ESD and leakage protection precautions have been taken.
2. Most failures in cryogenic amplifiers are produced when connecting or disconnecting the amplifier to/from the power supply. **A very careful procedure should be followed**.
3. Make sure that the power supply is **off** before connecting or disconnecting the power supply cable to/from the amplifier.
4. Make sure that the power supply and the amplifier are connected to the same protective ground before connecting or disconnecting the power supply cable to/from the amplifier.
5. Very especial care should be taken in case of a DC power supply floating respect to the protective ground. This produces most failures. It is safer to connect the **return** terminal at the output of the DC power supply to the protective **ground** permanently on the power supply side. If this is not possible (for example to avoid ground loops with long cables), a provisional connection from the return of the power supply to the amplifier case should be **made prior to any connection or disconnection** of the power supply cable. Always make sure that there is no voltage between the return of the power supply and the protective ground (case of the amplifier) before connecting the power supply cable. The maximum allowed voltage will be 0.020 Vrms measured with a high input impedance (> 10 MΩ) voltmeter in AC mode.
6. The power supply should have adequate built in protection to avoid excessive voltage and currents in the transistors in case of power supply failure and during the transients produced when the power supply is switched on or off. Adequate Zenner diodes can be used in parallel with the outputs, and adequate series resistors in series. If the protections are designed adequately, the amplifier will survive even in case of errors in the connections of the cables.

Storage of the amplifiers

1. The amplifiers should be stored in a clean dry anti-static environment.
2. The amplifier should be stored with short circuits in the power and RF connectors.
3. For permanent storage desiccators with less than 20% relative humidity should be used. The preferred method of storage is in dry nitrogen containers.
4. For transportation, and for short-term storage, anti-static plastic bags with silica gel bags to keep low relative humidity should be used.