Effect of Source Bonding Wires in HEMT devices: Probe Station Measurements

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1. Introduction

This report presents the results of the measurement of several types of HEMTs including the effect of bonding wires. The objective was to asset the accuracy of the models used for the design of cryogenic amplifiers. The measurements were carried out in a Probe Station in the 0.250-110 GHz frequency range at ambient temperature using the new equipment available in Yebes. The most interesting finding of this work is the resonances which appear at high frequencies (typically >50 GHz) and that were not predicted by the simple models based on equivalent circuits obtained by fitting on-wafer measurements of S parameters of the transistors plus ideal inductors to simulate bonding wires to the chip. These resonances can be explained by the parasitic capacitance of the source metallization and bonding pads of the transistors which is not usually included in the equivalent circuit. This effect appears at high frequency and does not affect much to the S parameters below 20 GHz, but can be dramatic at higher frequency, since it can produce oscillations, making the transistors virtually unusable in some cases.

2. Equipment

- Probe station mod. MPS 150 (Cascade Microtech)
- Coplanar probes mod. ACP 110-A-GSG-125 (Cascade Microtech)
- Vector network analyzer mod. PNA-X 5247 (Keysight)
- Millimeter wave controller mod. N5261A (Keysight)
- Millimeter wave heads mod. N5250CX10 (Keysight)
- Power supply mod. N3280A (Agilent)
- Transitions from coplanar to microstrip mod. ProbePoint 0503 (Jmicro)
- Coplanar calibration substrate (ISS) mod. 104-783A (Cascade Microtech)
- Microstrip calibration substrate mod. CM05LX (Jmicro)

3. Calibration

The chip measurements were taken with a standard LRRM calibration with the Cascade Microtech calibration substrate (Impedance Standard Substrate, figure 3) using WinCal software. With the standards used this calibration performs reasonably well in all the 250MHz-110 GHz range used. It was verified with an open (probes in air) and with a long matched coplanar line (~27ps) in the ISS substrate. The ISS was used in combination with an absorbing ISS holder (SN 116-334) as recommended by Cascade.

A microstrip calibration with the Jmicro calibration substrate (figure 2) and the multiline TRL (NIST type) algorithm implemented in WinCal was attempted, but it was not possible to calibrate over 90 GHz due to the limitation of the minimum line length in the Jmicro substrate. However, the microstrip lines over 5 mil alumina still perform reasonably well up to 110 GHz, as checked with measurements of the Jmicro thru (calibrated with the Cascade ISS in the coplanar reference plane). Finally, it was decided to take the microstrip measurements with the coplanar LRRM calibration but de-embedding the effect of the two coplanar to microstrip transitions. This was performed with a built-in feature of the PNA-X which allows de-embedding circuits characterized by their S-parameter files. Appendix I contain some information of the models used to generate the files used for de-embedding.

4. Measurements

Different types of devices were tested with and without bonding wires with a bias point near the optimum expected for minimum noise at ambient temperature. The details of the results of the measurements and of the parameters of the models of the equivalent circuits are shown in Table I and Appendix II. The measurements without bonding wires were taken with the chips on the Gel-Pack box used for storage. It was attempted to measure the chips mounted in the brass plate with the coplanar to microstrip transitions in place but without bonding wires. However, that measurement was not good since there was a strong coupling of the coplanar probes and the adjacent microstrip lines (transitions) terminated in open circuit. This appeared in the S parameters as a resonance which spoiled the measurement.

In the case of ETH 150 end ETH 50 devices, the chip measurements were compared with the equivalent circuit provided by ETH which includes pad parasitic elements obtained by measurement of dummy structures. The new measurements agree very well with ETH model predictions. Note that the maximum frequency used initially by ETH to fit the model parameters was 40 GHz and the new measurements are taken up to 110 GHz. Obviously a better result could be obtained by tuning some equivalent circuit parameters to fit the new data but it was preferred to leave the original values to illustrate the small difference. The chip equivalent circuit parameters are kept unaltered for the comparison with the measurements with bonding wires. Only the values of Lg, Ld and Ls are re-optimized to fit the measured data. In addition, a source pad capacitor (CpadS in figure 1) is introduced in an attempt to simulate the resonances found in the measurement.

Not such an elaborated chip equivalent circuit was available for the HRL 150 or the IAF 150. The HRL chip could be measured on the Gel Pack and the values of the equivalent circuit parameters were obtained by fitting to the measurements in the 0.25-110 GHz range. The IAF 150 is a smaller chip with a pitch of 100 um, and could not be directly probed in the present setup (configured for 125 um pitch). The equivalent circuit parameters of the IAF 150 device were obtained by fitting to the data obtained with three bonding wires on each side.

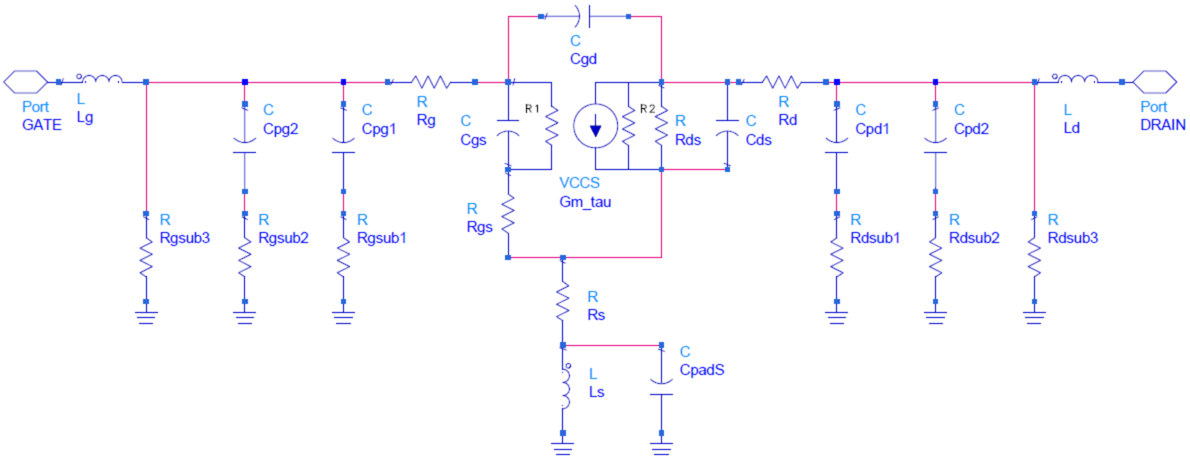


Figure 1: Equivalent circuit used for the transistors including bonding pad parasitics. Note the presence of CpadS (Source bonding pad) which was introduced to model the resonances observed in the measurements with bonding wires.

5. Conclusions

In the results presented in Appendix II is clearly visible the problem which appears due the resonance of the parasitic capacitance of the source pads with the bonding wires. Table I shows the values of the parasitic capacitance extracted from the measurements. The fitting of the models to the measured S parameters is far from perfect, especially above the resonance. Nevertheless, the qualitative behavior is more or less predicted by this simple model. Attempts to improve the fitting with more complex topologies did not succeed in obtaining a better result.

The relative values of the source pad parasitic capacitance obtained (Table I) are in agreement with what one would expect from the geometry of the transistors and pads. For example, ETH 150-1 and ETH 150-2 are identical in everything but the height of the chip and the capacitance scales (inversely) in almost the same factor as the height (~2). The highest value of parasitic capacitance is obtained for the IAF 150 HEMT which is the one with the smaller chip height. Looking at the photos of the devices it seems clear that the larger area of source pads corresponds to the ETH layouts. This suggests that the performance of these devices (respect to resonance with bonding wires) could be improved by modifying the layout, reducing the source metallization area as much as possible. The HRL 150 is the device in which the resonance effect appears at higher frequency. Coincidentally it is also the device with a smaller layout. This could explain the remarkable stable performance of the HRL 150 in cryogenic amplifiers, although it is true that the low value of transconductance also helps in this.

The ETH 50 is particularly problematic since it becomes clearly unstable ($|S_{11}| > 1$) with bonding wires for frequencies above the resonance. It will be difficult to use this device in a cryogenic amplifier unless an extremely low source inductance of the bonding wires can be obtained in the final configuration. Note that in present measurements, even with three short bonding wires on each side, the device is marginally unstable. More tests are needed to check whether an inductance low enough can be achieved to avoid this effect in a practical configuration.

TABLE I

Parameters of the equivalent circuit of the transistors measured

		ETH 150-1	**ETH 150-2**	**ETH 50**	**HRL 150**	**IAF 150**	
Gate Width (um)		150	150	50	150	150	
Chip Height (um)		~95	~170	~120	~120	50	
REF		T-245	T-273	T-317	T-78	T-315	
Vd (V)		0.5	0.5	0.5	0.75	0.5	
Id (mA)		15	15	5	15	15	
PAD PARASITICS	Cpg1 (pF)	0.0162	0.0162	0.0146	-	-	
	Cpg2 (pF)	0.0006	0.0006	0.0070	-	-	
	Rgsub1 (Ω)	14.1	14.1	10.3	-	-	
	Rgsub2 (Ω)	42K	42K	98K	-	-	
	Rgsub3 (Ω)	392K	392K	90K	-	-	
	Cpd1 (pF)	0.0176	0.0176	0.0155	-	-	
	Cpd2 (pF)	0.0009	0.0009	0.0013	-	-	
	Rdsub1 (Ω)	13.8	13.8	9.6	-	-	
	Rdsub2 (Ω)	74K	74K	73K	-	-	
	Rdsub3 (Ω)	318K	318K	87K	-	-	
CHIP Eq. CKT	Rg (Ω)	1.9	1.9	0.6	0.3	0.3	
	Rd (Ω)	1.5	1.5	4.7	1.4	1.4	
	Rs (Ω)	1.2	1.2	4.7	0.5	0.5	
	Cgs (pF)	0.0984	0.0984	0.0276	0.1075	0.0805	
	Rgs (Ω)	3.8	3.8	7.9	2.9	3.1	
	Cds (pF)	0.0397	0.0397	0.0155	0.0471	0.0467	
	Rds (Ω)	59.1	59.1	148.2	83.62	50.41	
	Cgd (pF)	0.0288	0.0288	0.0112	0.0321	0.0431	
	Gm (mS)	187.5	187.5	62.1	129.9	162.3	
	Tau (ps)	0.064	0.064	0	0.079	0	
CHIP	Lg (nH)	0.0653	0.0653	0.046	0.0218	-	
	Ld (nH)	0.0528	0.0528	0.050	0.0250	-	
	Ls (nH)	0.0013	0.0013	0.0006	0.0051	-	
	CpadS (pF)	-	-	-	-	-	
3 BW	Lg (nH)	0.0993	0.1294	0.1159	0.1428	0.1054	
	Ld (nH)	0.1215	0.1614	0.1012	0.1258	0.1151	
	Ls (nH)	0.0413	0.0471	0.0513	0.0376	0.0256	
	CpadS (pF)	0.1470	0.0796	0.1196	0.1234	0.2020	
1 BW	Lg (nH)	0.1114	0.1297	0.1159	0.1168	0.1020	
	Ld (nH)	0.1107	0.1469	0.1012	0.1083	0.1073	
	Ls (nH)	0.0792	0.1062	0.1039	0.0758	0.0664	
	CpadS (pF)	0.1524	0.0700	0.1078	0.0929	0.1601	

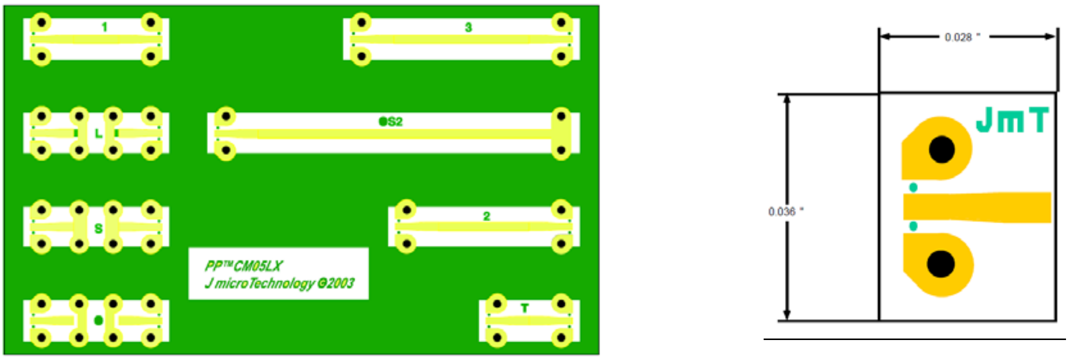


Figure 2: Jmicro coplanar to microstrip transition and calibration substrate. The frequency range of the NIST multiline TRL calibration is limited by the length of the shortest line to ~80-90 GHz.

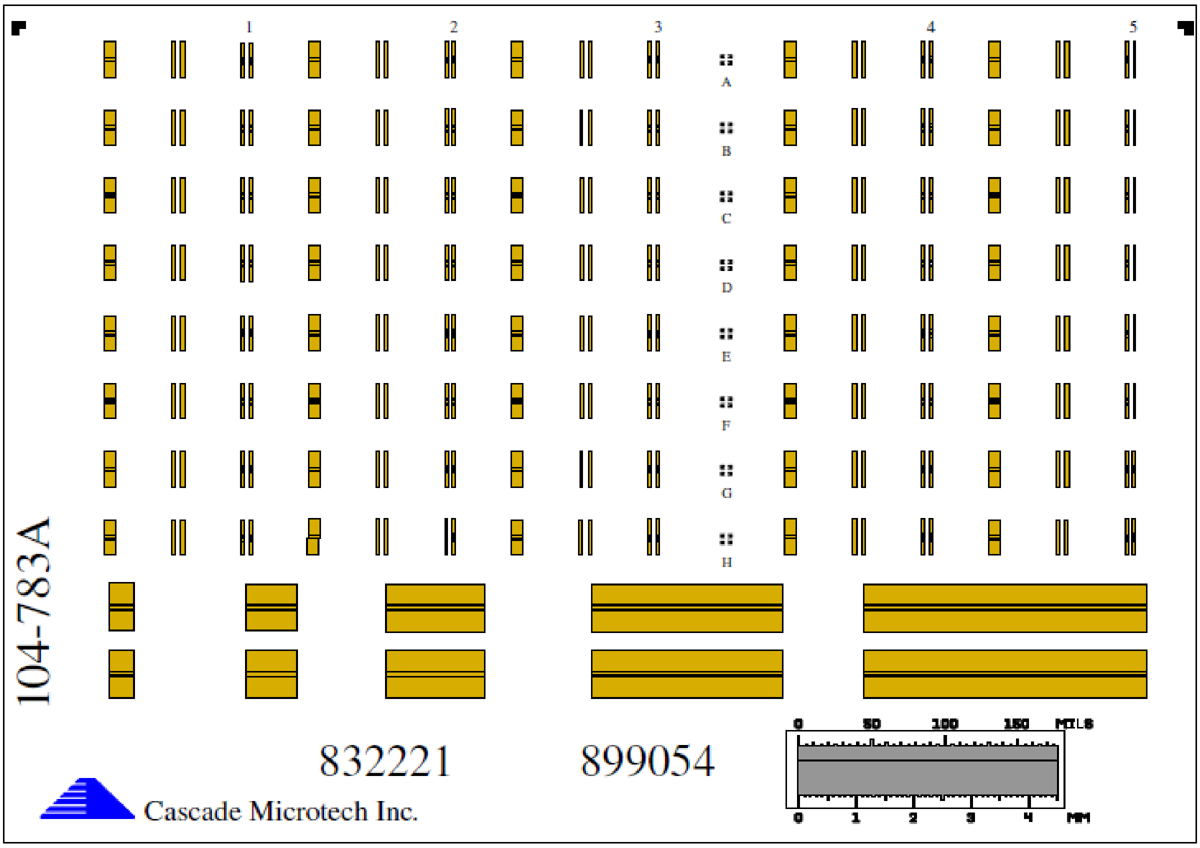
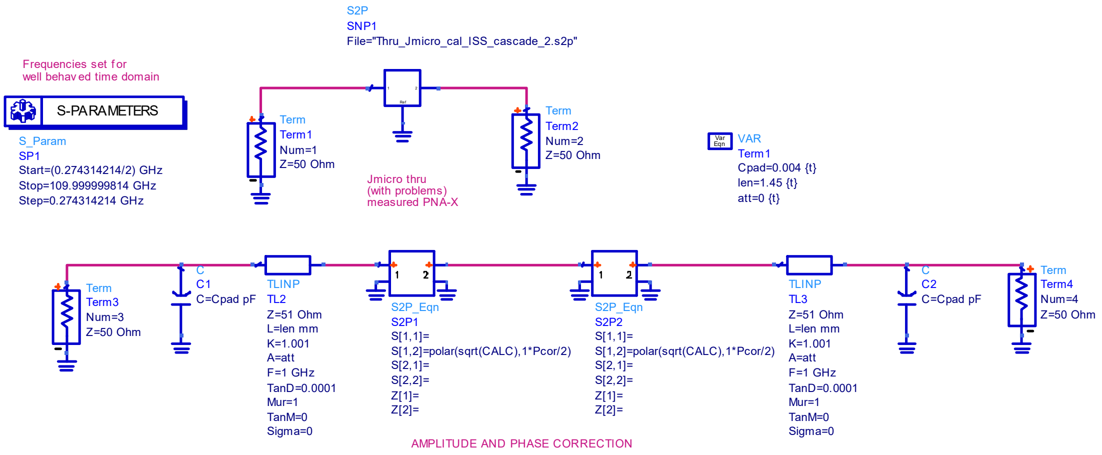


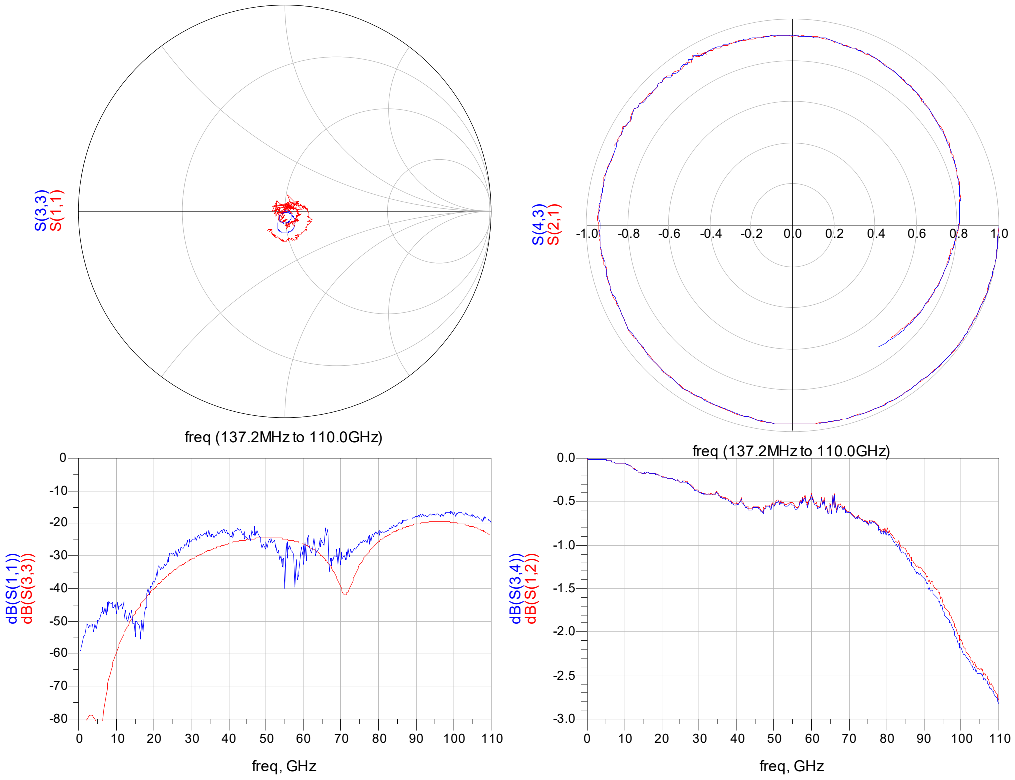
Figure 3: Calibration substrate used for LRRM calibration on the coplanar reference plane in the 0.250-110 GHz frequency range.

6. Appendix I

Model used for de-embedding J-micro coplanar to microstrip transitions.

(Half of the model is used to generate S2P files used for de-embedding)

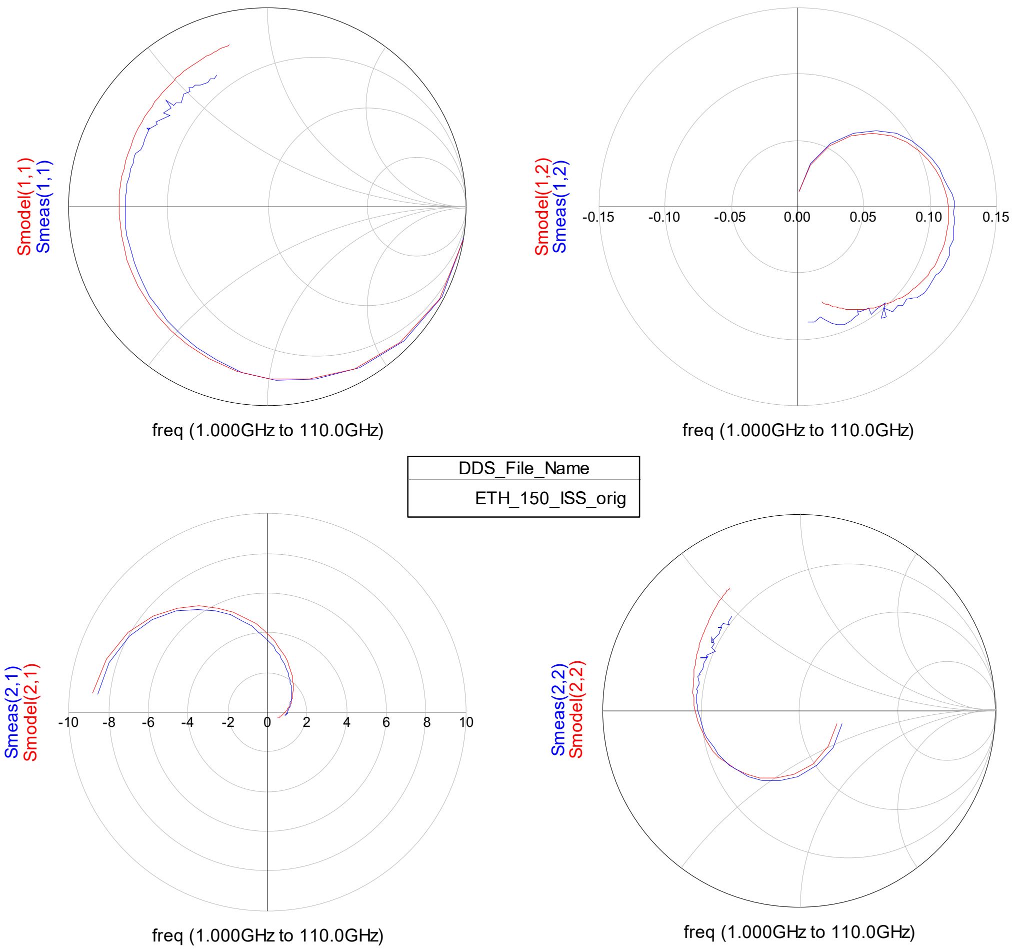




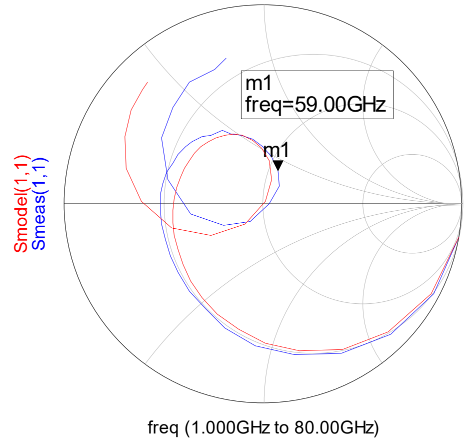
7. Appendix II

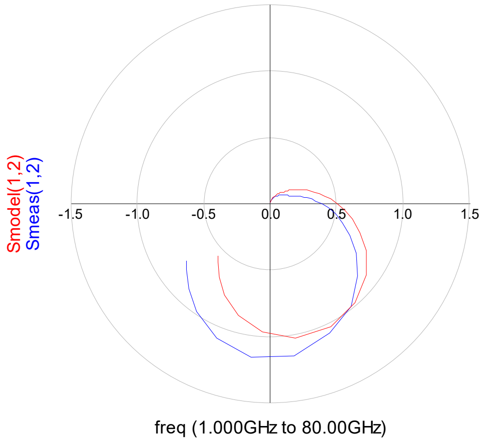
Comparison of measurements and models of the transistors tested.

ETH 150 (chip height: 95 um)



ETH 150 (chip height: 95 um) 3 BW each side





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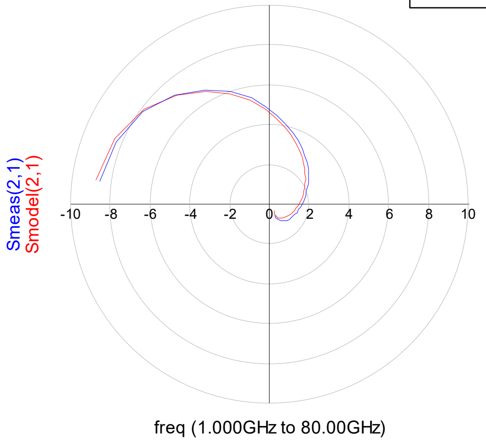
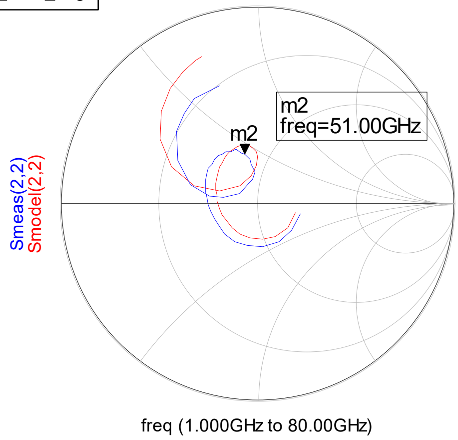
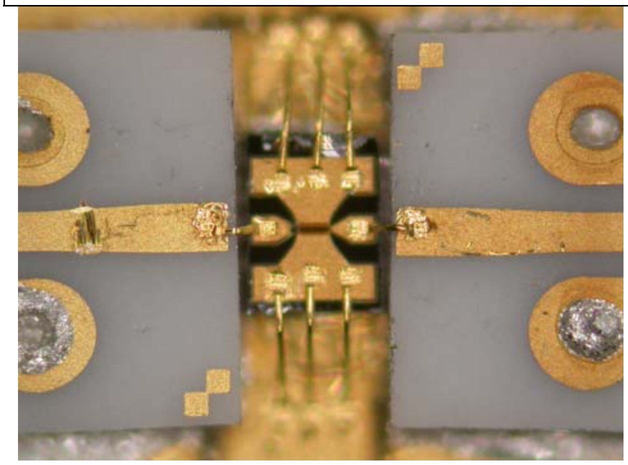
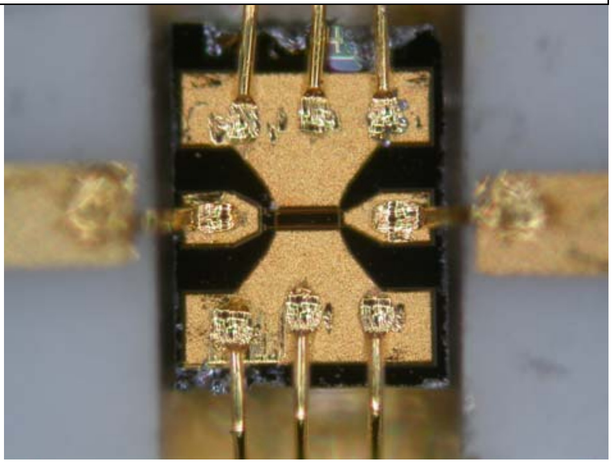
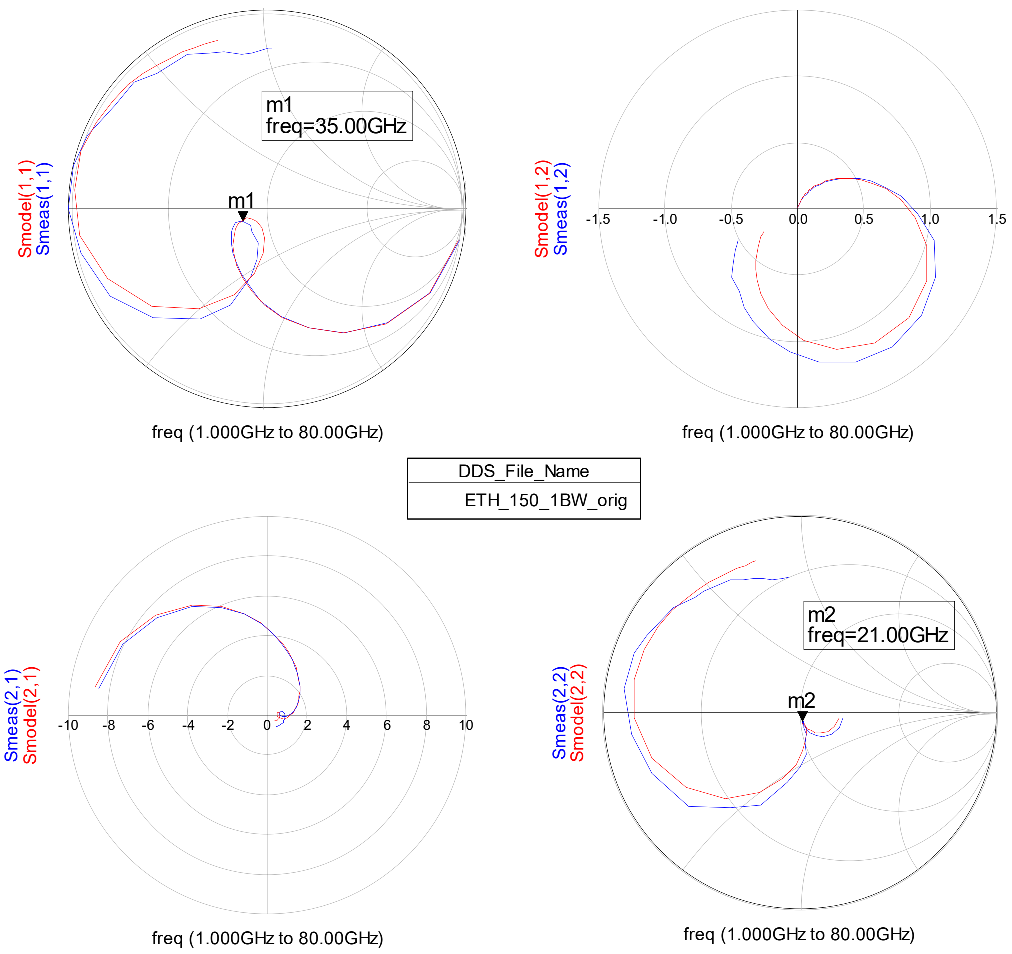


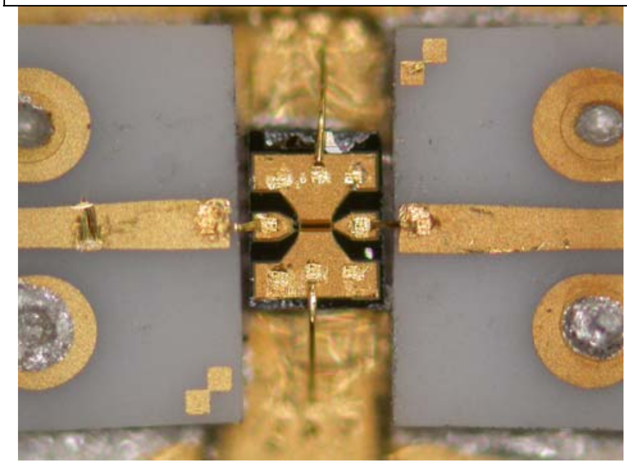


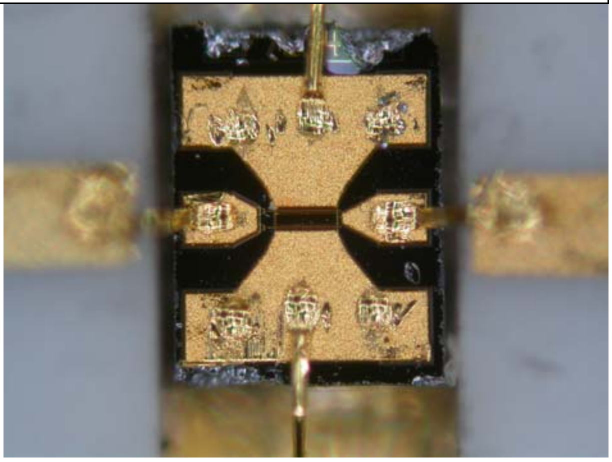




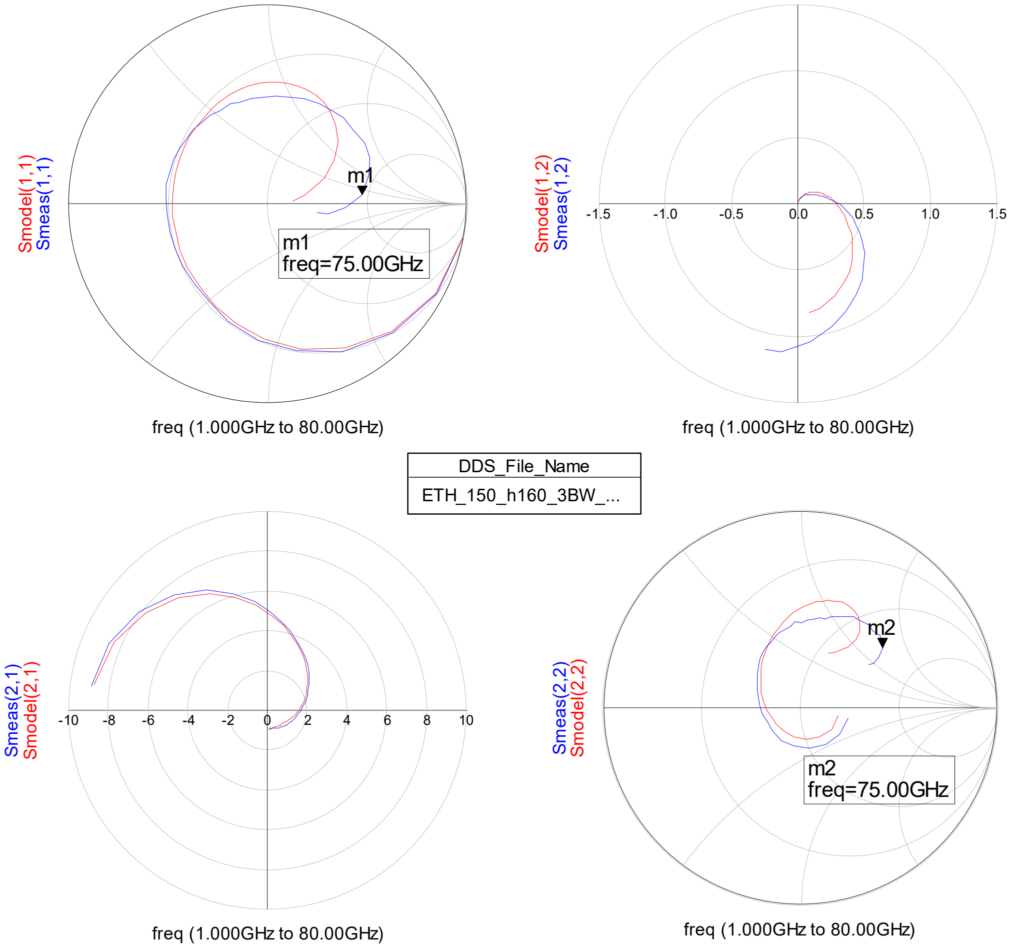
ETH 150 (chip height: 95 um) 1 BW each side

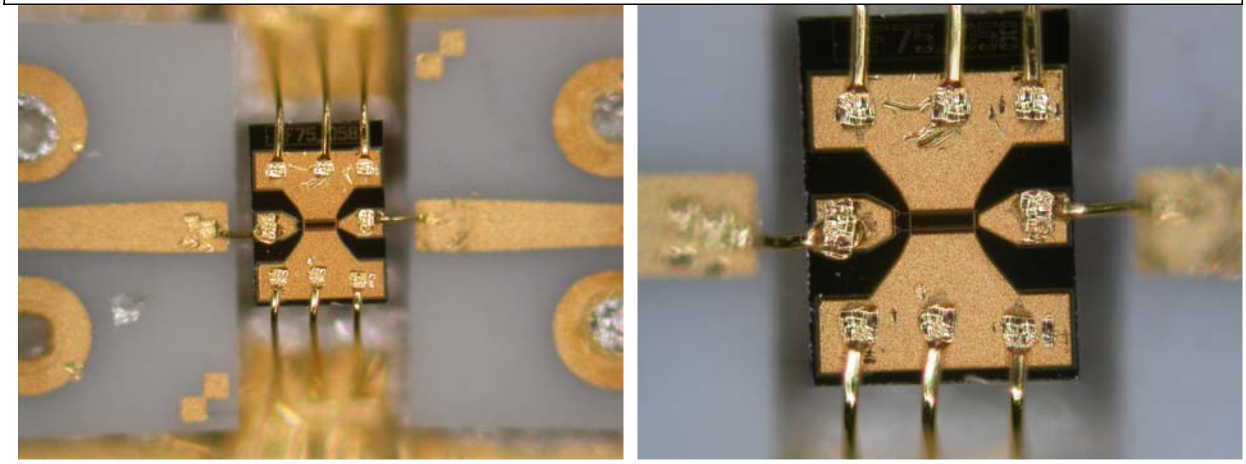






ETH 150 (chip height: 170 um) 3 BW each side





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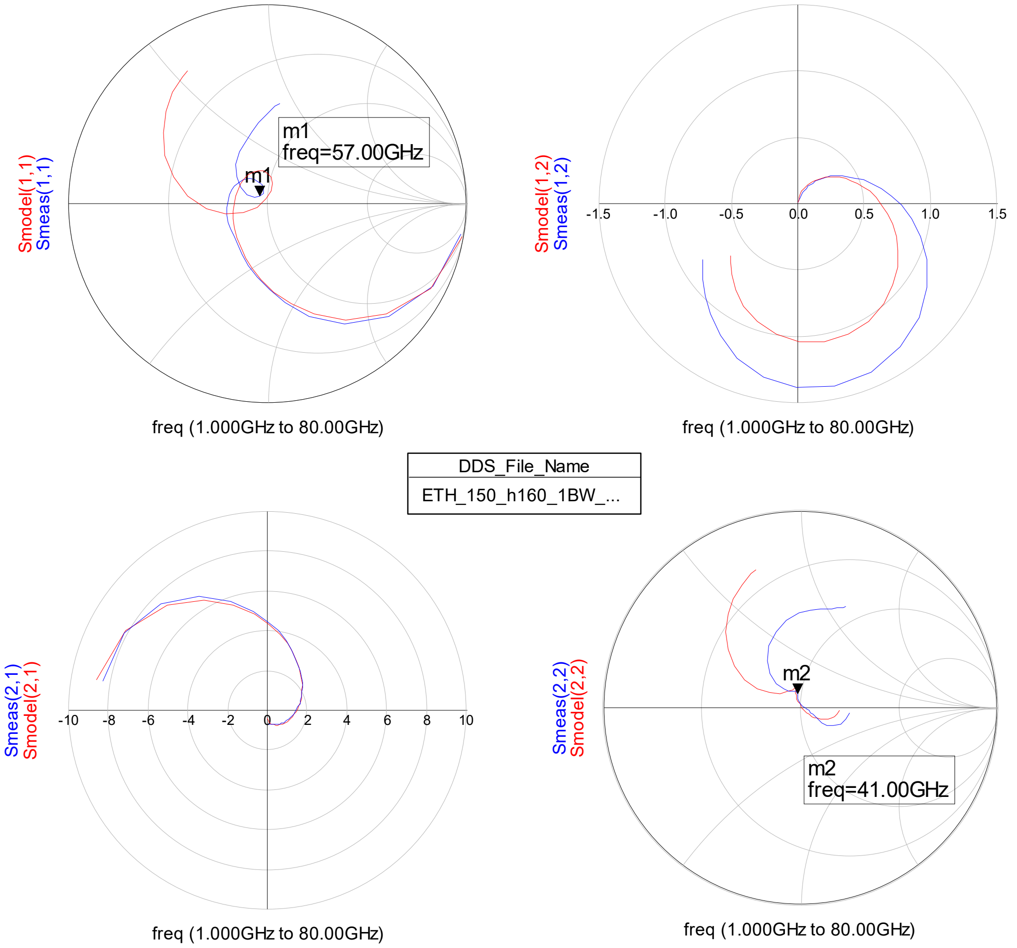

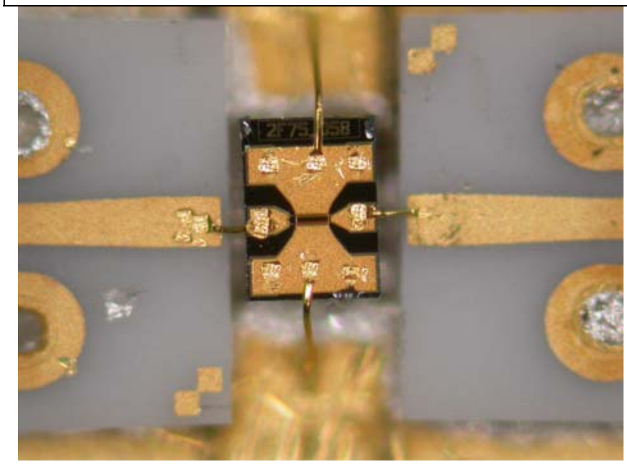

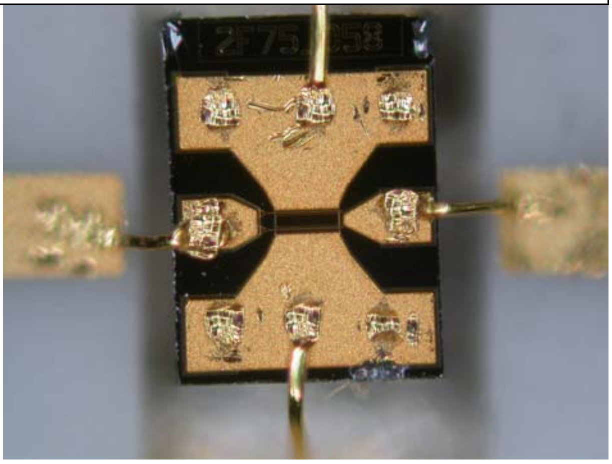

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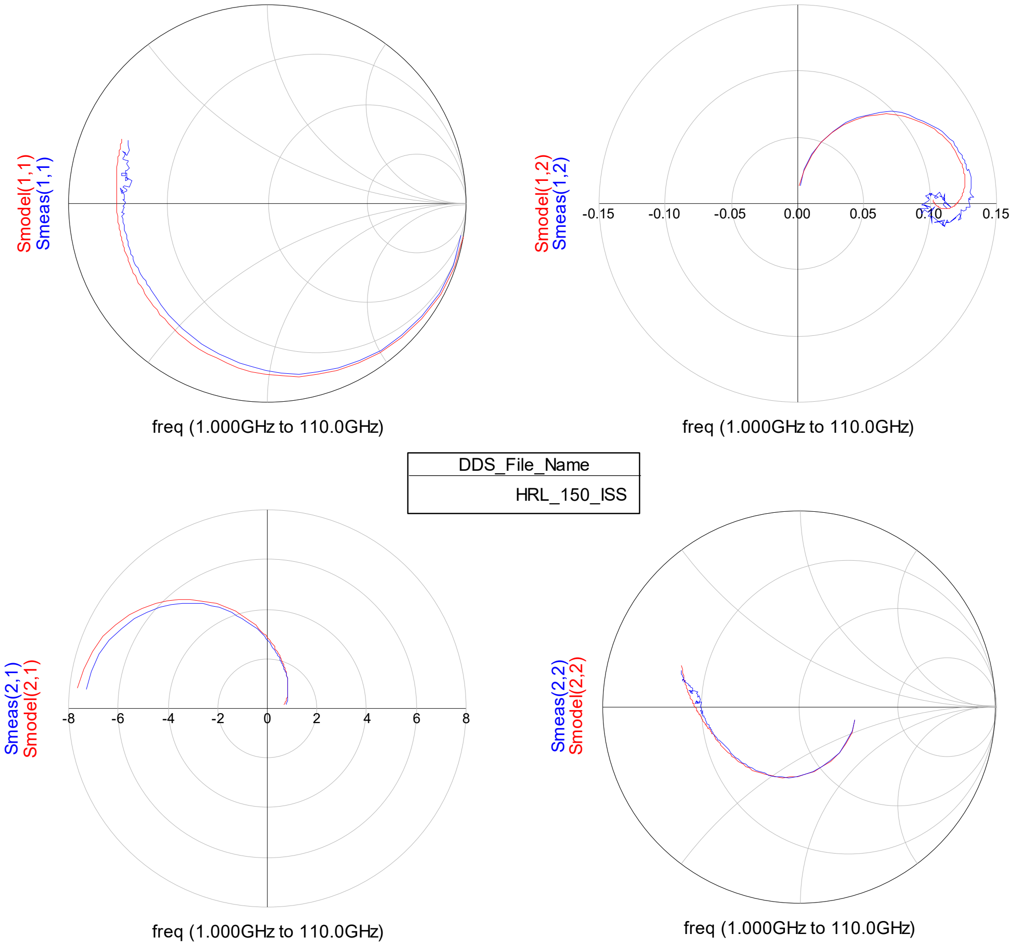

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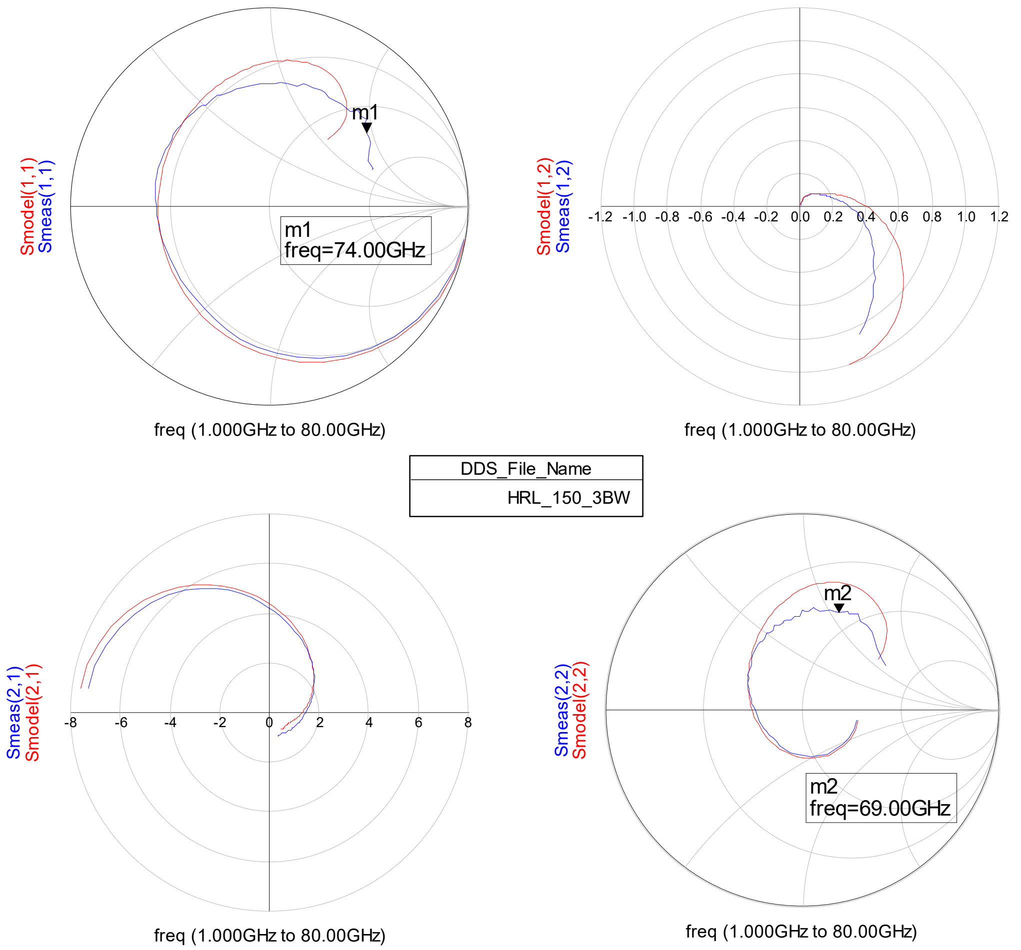

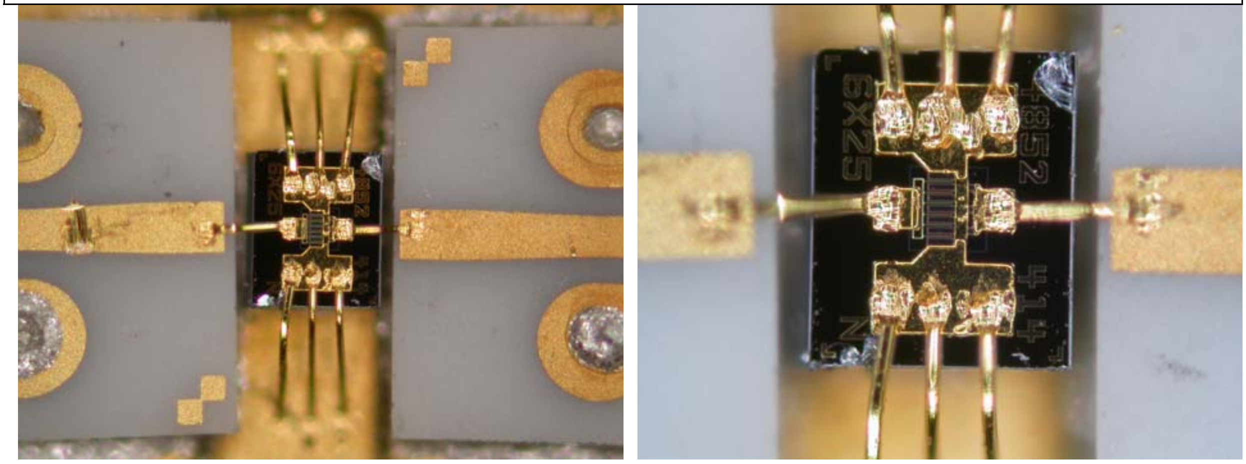

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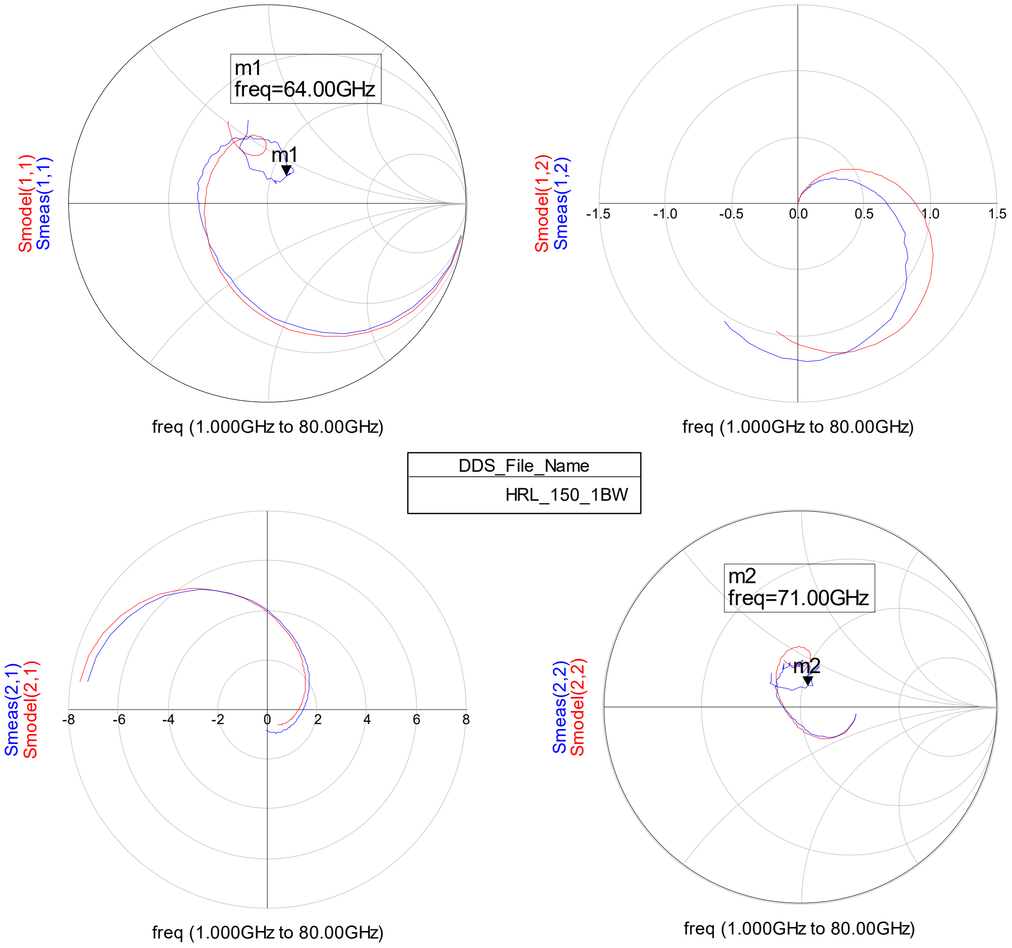

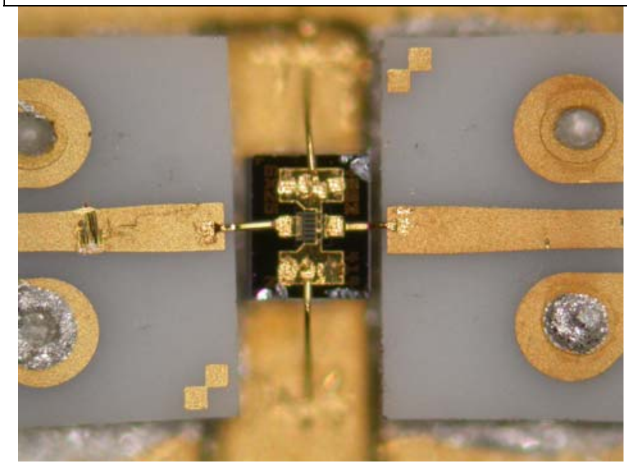

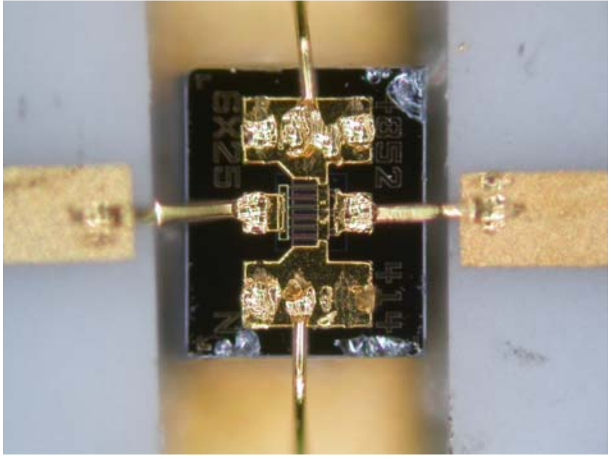

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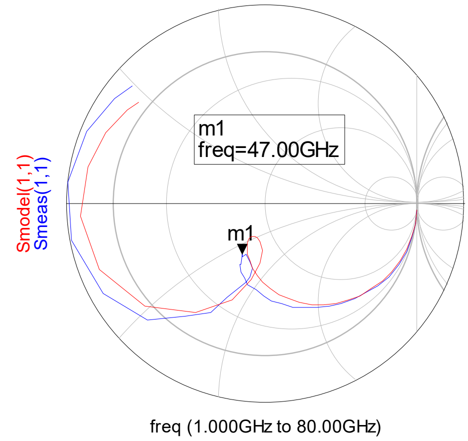

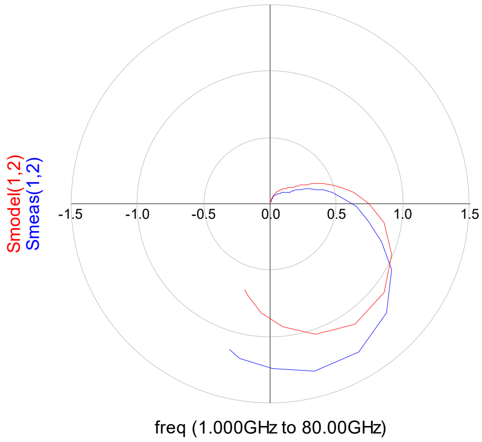

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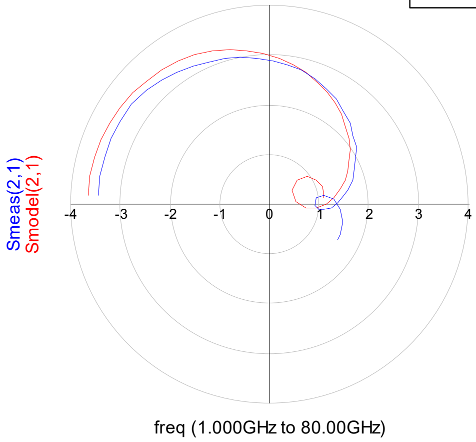

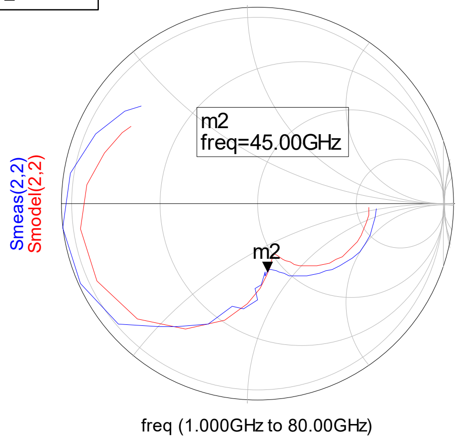

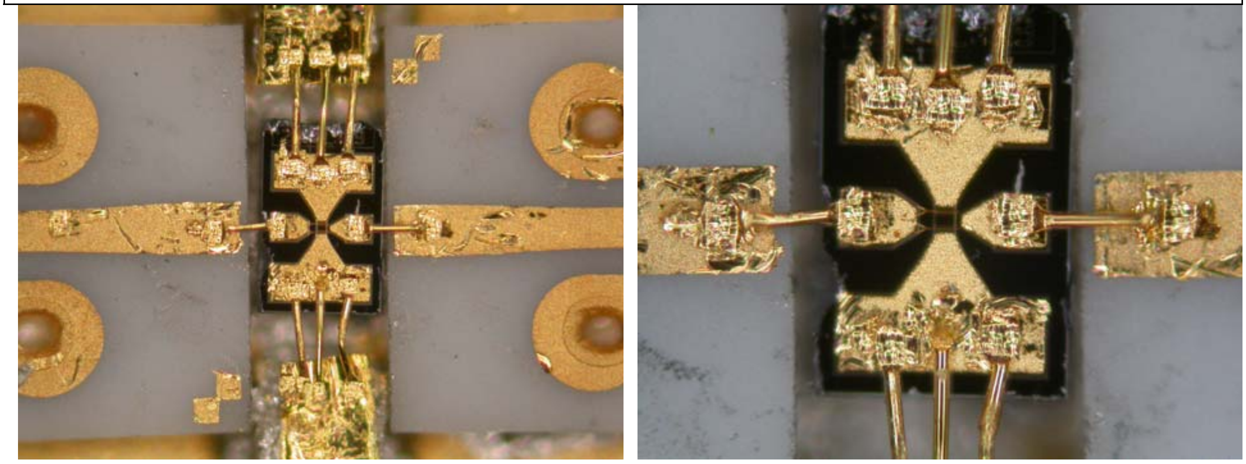

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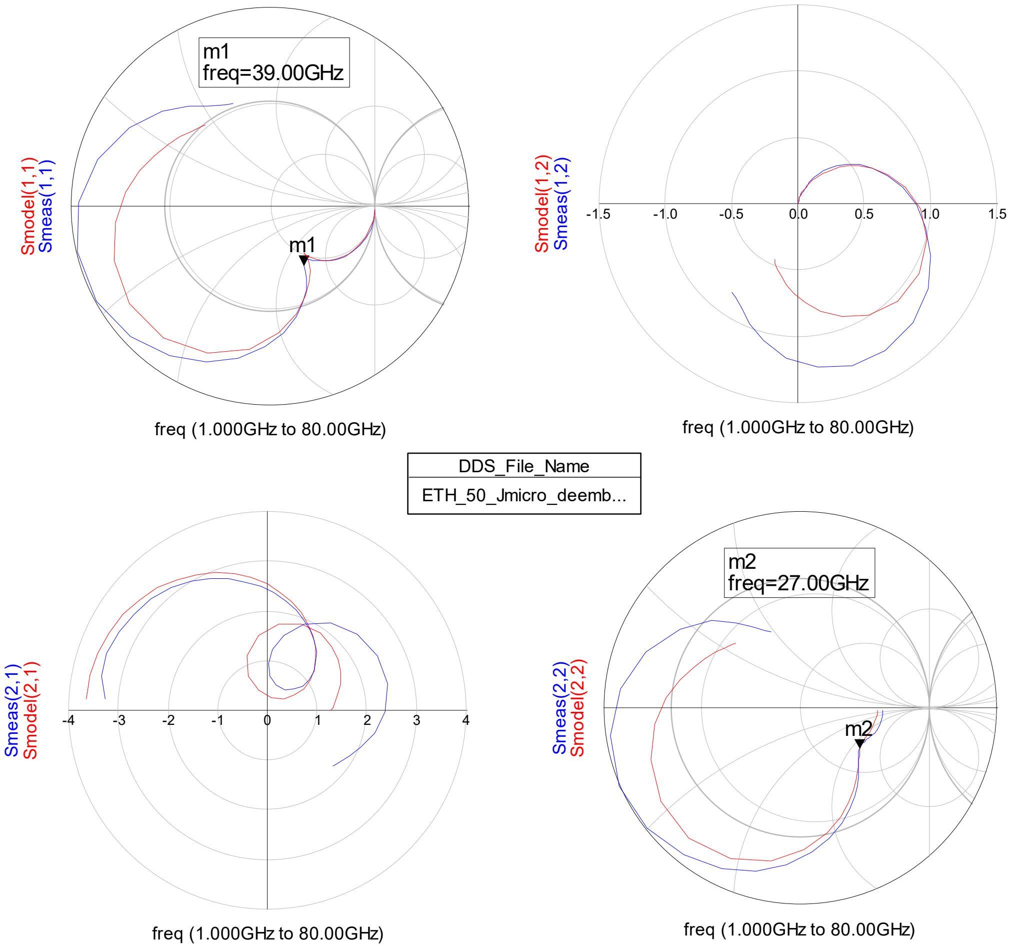
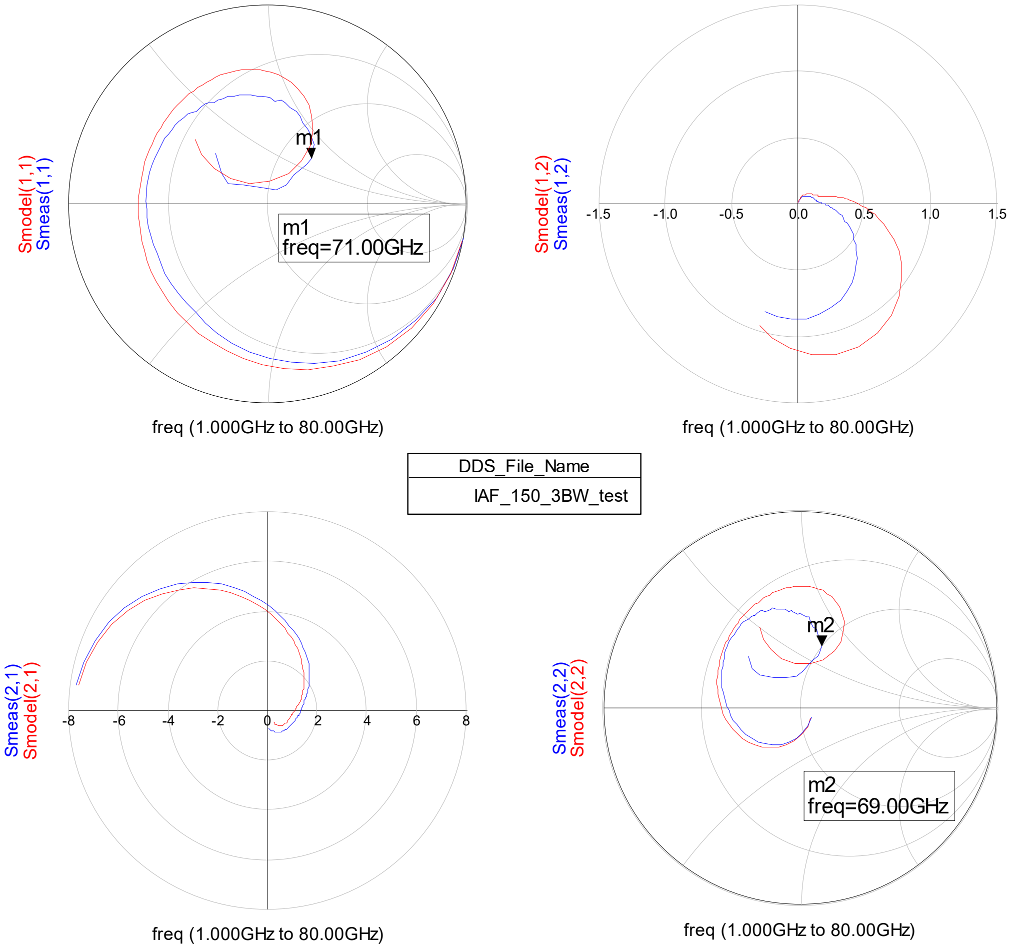
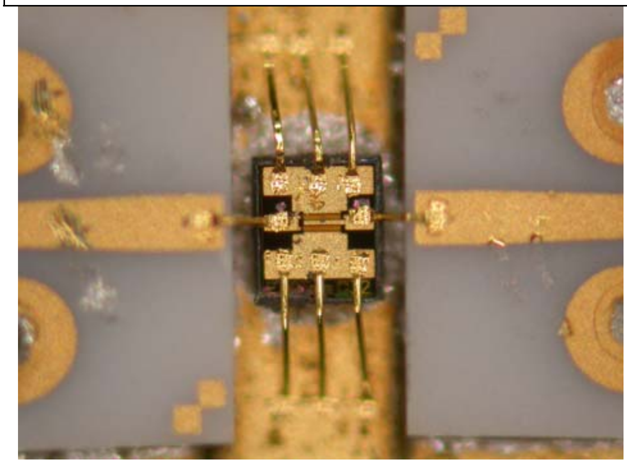
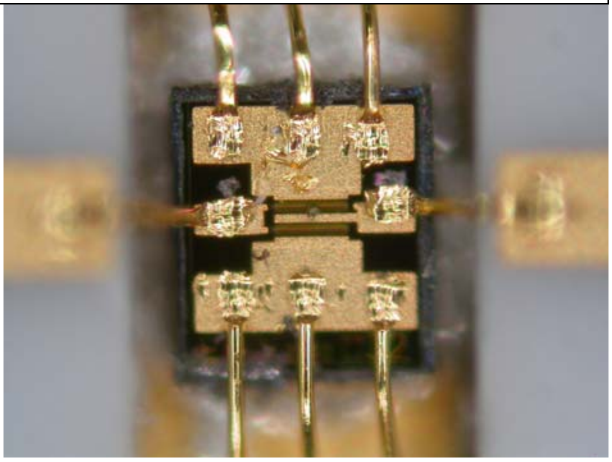


IAF 150 (chip height: 50 um) 3 BW each side







IAF 150 (chip height: 50 um) 1 BW each side