Hardware upgrades and validation of the Yebes DBBC (I)

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Revision history

Version	Date	Author	Updates
1.0	10-12-2013	P. de Vicente	Overlay, and sections: 1,2 and 3
1.2	14-02-2014	J. González	Rest of sections, and preliminary version
1.3	08-09-2014	J. González	Revision and section 9 update

Contents

1 Introduction

Two hardware modifications have been performed at Yebes in the DBBC to get a better functionality.

The first modification was done in the IF modules, also known as Conditioning Modules (CoMos) and its aim was to get an analog signal from the power detector at these modules. This modification was requested to the DBBC team by one of the authors of this report and it was designed by M. Wunderlich and G. Tuccari. This report describes the changes performed following instructions provided by M. Wunderlich. The goal is to use these detectors for total power continuum single dish observations since they provide a large dynamic range. The second modification was requested by the DBBC team to improve the behaviour of the COREs and reduce the system noise.

The system was checked after these modifications and validated to be used as a the standard VLBI backend in VLBI observations. These checks are described along the text.

2 IF modules upgrade

The DBBC has 4 independent IF modules, called CoMos (Conditioning Modules) that allow to work with 4 IFs (for example 2 pols and 2 IFs per pol) simultaneously. Each module has 4 SMA inputs which provide flexibility to use different setups avoiding to move cables from one connector to another. Each module only processes the signal from one connector at a time. Input connectors are selected using an internal switch and software commands.

The CoMos filter the signal, detect the total power and implement an automatic gain control by adjusting attenuators inside. These modules have evolved with time and several versions are already available. Our CoMos are Unica 2 version and as such only have two filters: 10-512 MHz and 512-1024 MHz. During normal operations Yebes 40m telescope uses filter 2 (512-1024 MHz).

Before the filters there is a gain control which allows to produce a constant output power for the next module in the chain (ADB boards). The attenuator can be controlled automatically or manually in steps of 0.5 dB between 0 dB and 32 dB, which for the user corresponds to values between 0 and 64 arbitrary units respectively. The power detection is done afterwards by an integrated circuit (Hittie HMC610LP4) which generates a DC voltage signal whose amplitude is proportional to the power in the band and ranges from -2.45 V to 2.45 V. The detection is therefore quadratic-law type. The working input power ranges from -48 dBm to -3 dBm in 500 MHz which after being digitized with 16 bits, is converted to arbitrary units between 500 and 64000. The signal is read outside the CoMo, in the PCI 9111 board where the automatic gain control is controlled for an optimum power level for the ADB modules. The required attenuation is calculated and applied to the attenuators inside the CoMo .

Fig. 1 shows a picture of an Unica 2 CoMo board with labels that identify the two filters and the detecting power circuit. Three 3 dB splitters are also visible, although not tagged. The connectors on the right (TP out and IF out) are used internally to send the signals to other modules. The gain control is not visible on the board and we believe it is between the first 3 dB splitter and the switch at the input of the filters. The IF signal, once its level is adjusted to the

optimum level, is sent via the ”IF out” connector to the ADB module.

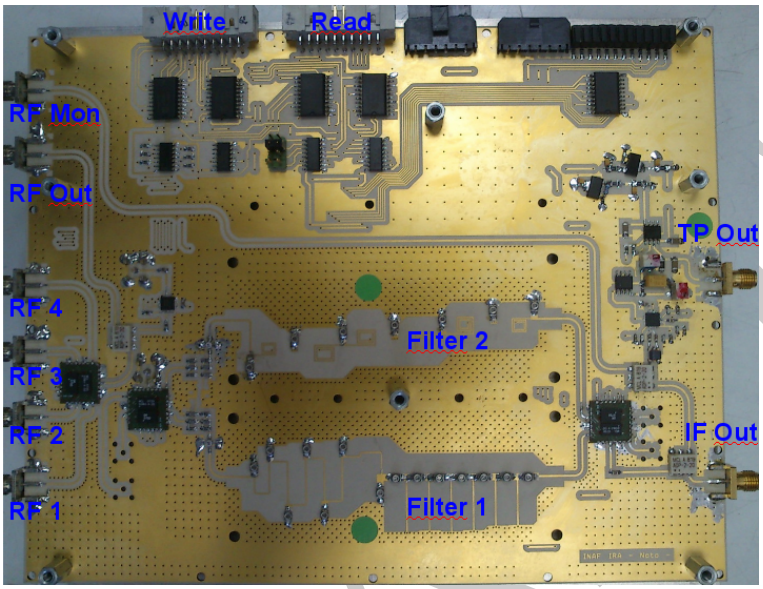


Figure 1: *CoMo board (Unica 2 version). The detection power circuit is in the upper right corner of the board (to the left of the green dot sticker)*

Two SMA connectors labeled “RF Mon” and “RF Out” are available in each CoMo. “RF Out” is a half power copy of the input signal, “RF Mon” is a copy of the signal that goes to the ADB (Analog to Digital Board) with a power 9 dB lower than the input signal. These power level differences arise from the three splitters. The monitored signal has been filtered and its power level adjusted according to the automatic or manual gain control. Fig. 2 shows a scheme of the signal flow in the CoMos as described previously once the modification was implemented.

The modification consisted on obtaining a buffered copy of the analog signal produced by the integrated circuit and sending it to a BNC connector on the external plate of each CoMo. The reason for using a buffered signal is to prevent that an external short in the cables could stop the total power monitoring. M. Wunderlich designed a small PCB board which implemented this buffered output. The PCB is glued to the main board and connected with some cables to the board and to the external BNC connector.

Fig. 3 is a picture of the modifed board. The PCB was attached to the main board using two sided tape.

Finally, the linearity of the detection circuits was tested using a similar procedure to the one explained in [6]. We injected AWGN noise to each of the four IF channels and manually commanded the attenuation in every channel, using steps of 1 dB. We measured the signal from the 4 outputs by injecting them to the Pocket Backend, an ADC used nowadays in single dish observations. The voltage of the detected signal varies from 1.68 (40 dB attenuation) to 2.18 volts (0 dB attenuation). The digitalized detected power shown by the PBE is in arbitrary units.

This figure shows small differences between detectors. The transfer function gradient is similar for IFs B, C and D and slightly lower for IF A. Despite of this, the linear range is very approximate to 36 dB for every detector.

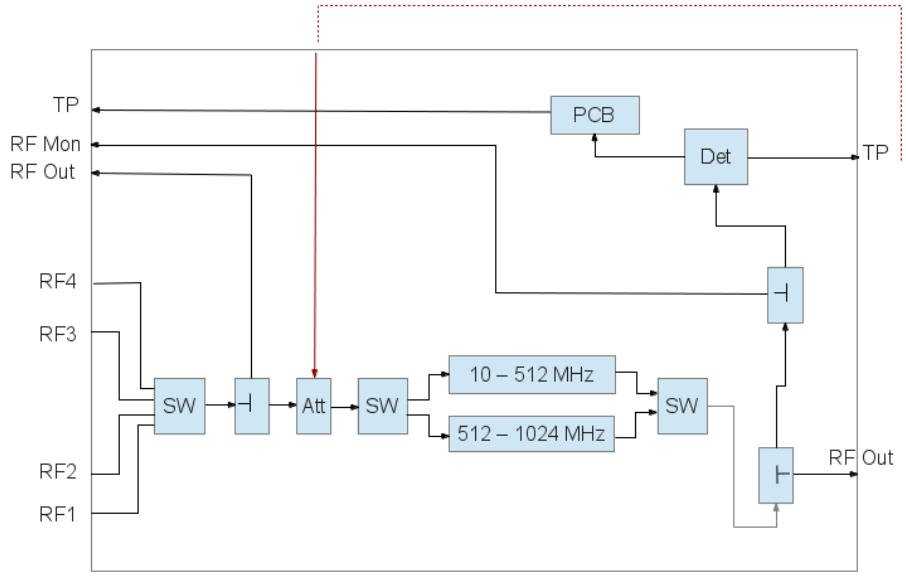


Figure 2: *Probable schematics of the Unica2 CoMo module. The modification is already included: the PCB board and the BNC connector are visible*

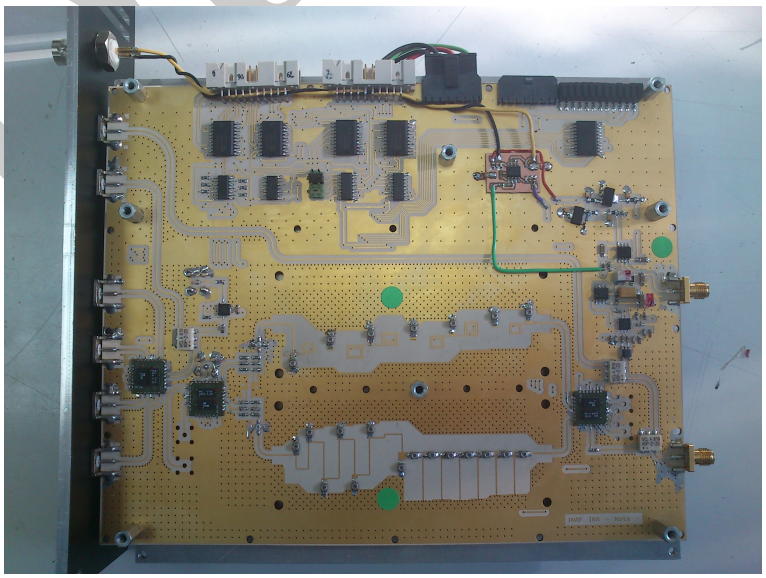


Figure 3: *Modified Unica 2 board in the CoMo to obtain a buffered copy of the analog signal from the total power detection*

3 Modification in the ADB boards

It was discovered that a difference between power levels in the ADB and CORE boards caused an increase of the system noise. This is described by M.Wunderlich in [2]. By correcting this effect, the noise is reduced and the range of input power levels at which the system works better is larger. Before the modification the power level at which the system works best (high SNR and linearity) was close to 38000 counts. It is expected that with this modification the range of input power values will be wider.

This modification allows to remove from the bus the interface boards between the ADB and the COREs. The consequence is that the bus is smaller and fits in a smaller space allowing for more elements and the signals along the bus travel a shorter path, which probably improves the quality of the signals in the last COREs. de Vicente & González (2013) showed that the range of linearity in DDC and PFB mode for COREs 3 and 4 was smaller than with COREs 1 and 2.

The modification consisted on reducing the supply voltage of the digital electronics by 0.5 V. This is achieved inserting a Schottky diode (1N5819) in the power plane. A part of the plane has to be removed to ensure that the only connection between both areas is done via the diode. The two areas are created by milling away the first layer of the multilayer board. At Yebes this was done with a cutter. Fig. 4 shows the milling and the diode connecting both areas.

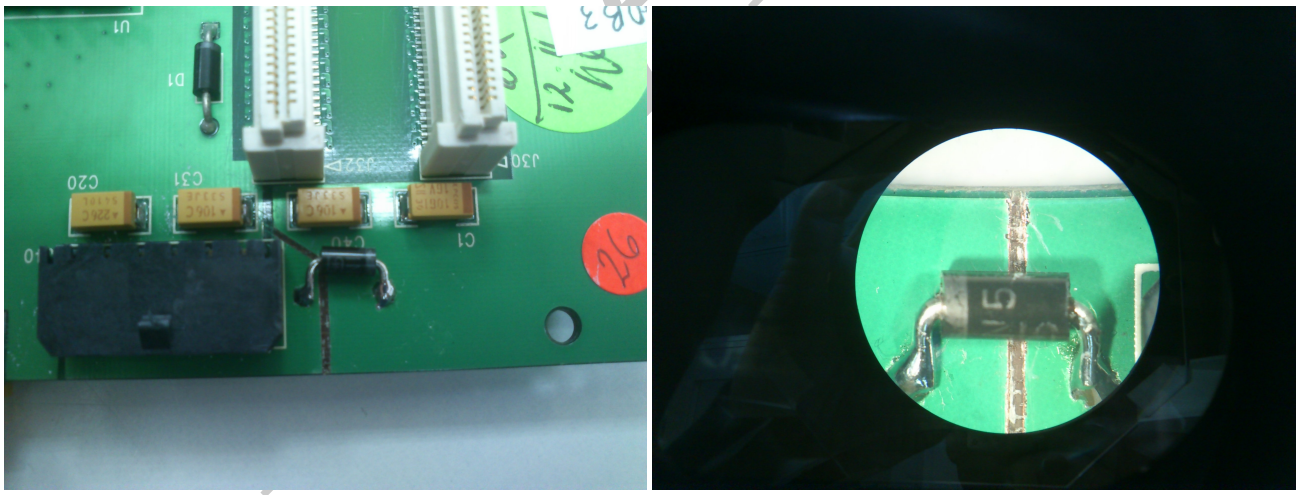


Figure 4: *Milled channel and diode connecting both areas in the ADB1.*

The second required modification consisted on modifying the location of one of the legs of the clock driver circuit. The leg was soldered on a different pad so that the circuit uses a different supply voltage. Fig. 5 shows a picture of the modification in one of the ADB1s.

With these modifications, the interface boards that connected the CORE with the ADB must be removed. Some power supply cables can be taken away to unclutter the space. Fig. 6 shows a picture of the BUS before and after the modification. The interface boards have disappeared in the newer picture.

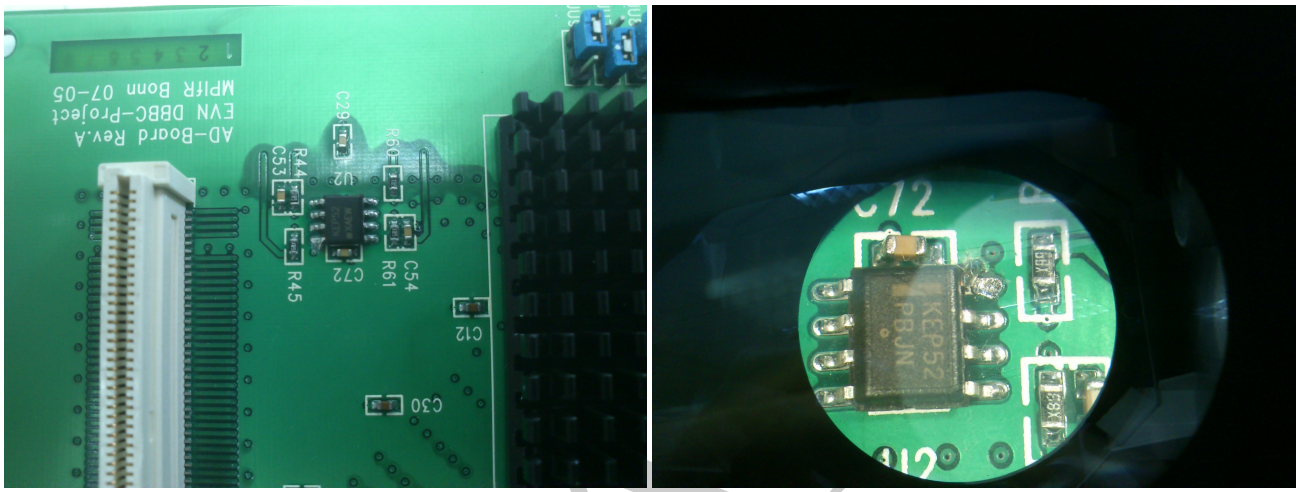


Figure 5: *Clock driver circuit in which one its legs has been unsoldered and soldered in a different position.*

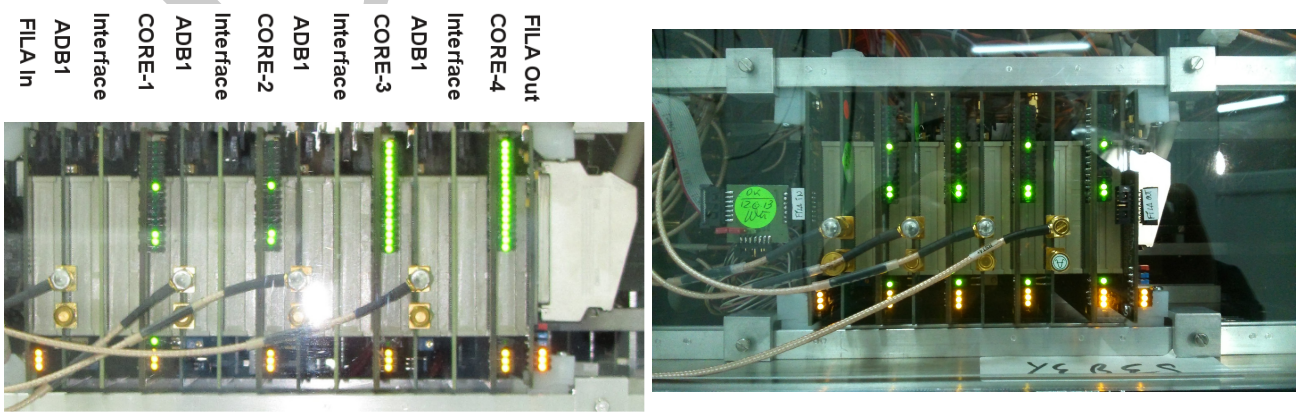


Figure 6: *View of the old (left panel) and new (right panel) bus in the DBBC.*

4 Hardware update in Bonn and assembly

After the modifications described above the system was tested. It was found that the four COREs did not synchronize correctly to the external PPS. However if the system worked with only the first two COREs the synchronization was correct. This behaviour was determined just by setting the DBBC in DDC mode and inspecting the LEDs in the front side of the COREs. In the DDC mode LEDs 16th and 10 of all boards should blink at the same time. LED 16th is associated to the internally generated PPS while LED 10th lights with the external PPS. If there is some delay along the bus LEDs will blink out of sync after some minutes or even some hours.

Since the DBBC did not work correctly the DBCC was sent for inspection and repair to Bonn where it was found that synchronization problems involving last Core2 modules could be due to swapped addresses on the two boards (the reader can find a picture of the switch that gives address to a board in figure 7). In addition to properly adjust the addressing switch several tasks were performed in MPIfR (Bonn).

- Replaced flash memory with hard-disk drive.
- Added remote power on/off option.
- Modified PCI7200 due to possible driver overheating problem.
- Replaced P945 Atom CPU with Advantec type to get rid of the booting problem.
- Modified FilaOut to overcome possible Mk5B grounding problem.
- Calibration of the Unica boards.
- Updating all software to the latest state.
- Replaced CaTset.

To prevent transport damages, the digital electronics stack was partly dismantled, and the system was reassembled in Yebes. Once assembled ($FiLa + ADB1_1 + Core2_1 + ADB1_2 + Core2_2 + ADB1_3 + Core2_3 + ADB1_4 + Core2_4 + FiLa$) a JTAG booster was needed at the beginning of the stack as shown in figure 8. This small PCB has two functions; it acts as a demultiplexer in case there is a FiLa10G embedded into the system so it can be programmed through just one USB port (this is not the case in Yebes), but it is also an amplifier for programming currents to the FPGAs since it was seen that in some cases the last boards in the stack did not receive enough power.

Two VSI interfaces are available at the last FiLa board allowing the user to reach 4096 Mbps. VSI1 is the connector nearest to the back, VSI2 is the one nearest to the front.

The PC motherboard replacement forces us to use a modified version of the VGA cable (DB-15 HD) because there is not enough space for this type of connector at the rear panel. Hat-Lab supplies this cable, but in Yebes it was necessary to use a female-female adaptor to integrate the system in the KVM switch.

The external references for the DBBC are 1 pps and 10 MHz, obtained from the Station Sync (VLBA terminal) and the local oscillator (Hydrogen maser through the Quartzlock distributor)

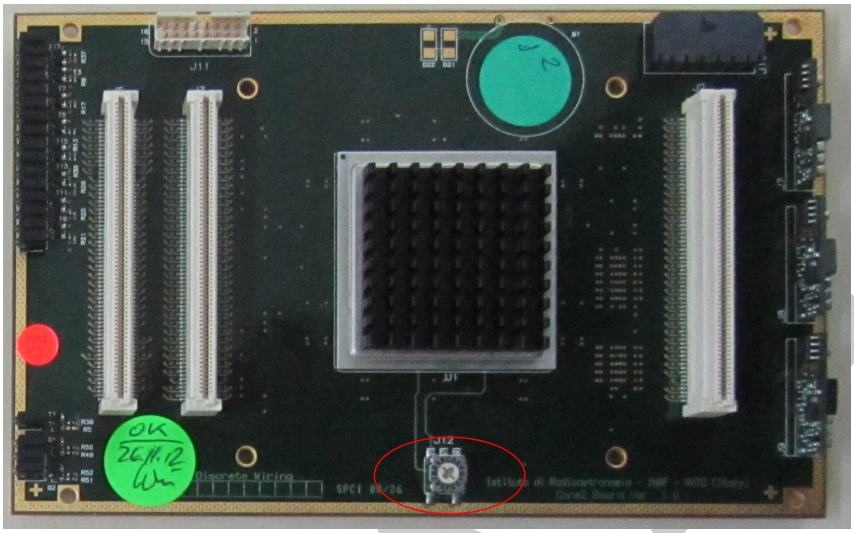


Figure 7: Core2 top view. This side faces the output of the stack. The address switch has been red circled.

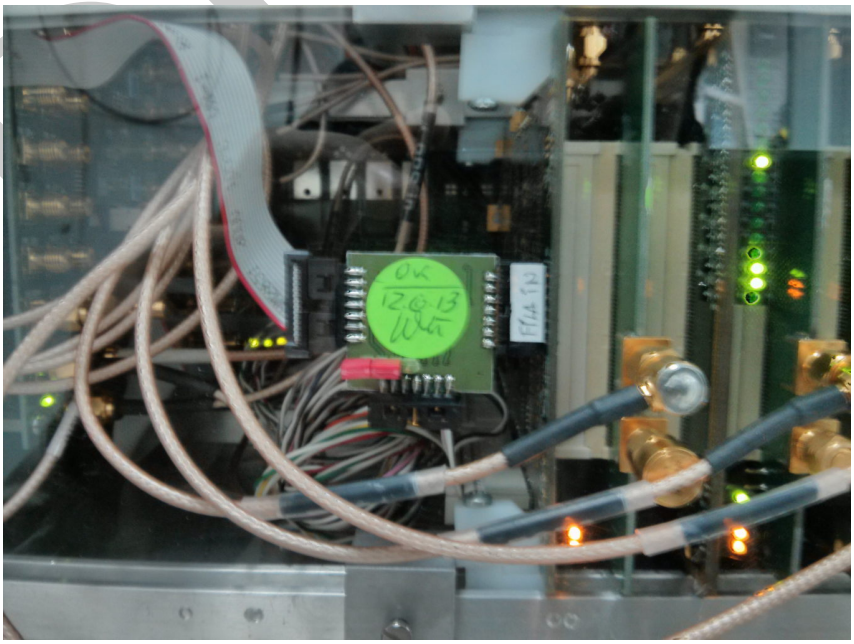


Figure 8: View of the JTAG booster through plexiglas during normal operation

respectively. It is recommended to install a 5 dB pad to achieve -10 dBm which is the nominal value for the 10 MHz reference. The DHCP server at Yebes was set up to provide IP addresses to the DBBC and to the FiLa10G.

Once the system was fully connected, a simple procedure [3] was run to check for properly behaviour of the equipment.

4.1 Analog electronics check-up

The conditioning modules can be tested injecting white noise between 10 and 1100 MHz and looking at the output using a spectrum analyser. The DBBC includes an utility in the system called agc_if.exe that allows the user to change conditioning parameters (an alternative is to use typical observing mode commands. The output is available at the two SMA connectors labeled as **RF_out** and **RF_mon** which, as explained at the beginning of the report, provide copies of the input selected IF signal (3 dB down) and the ouput conditioned IF signal respectively. The four inputs and both filters per IF were tested and all behaved as expected.

4.2 Digital electronics check-up

The DBBC was set to DDC mode (version 104) and we followed instructions in [3] to test the electronics. The synchronization between the DBBC and the external 1 PPS (Station Sync) was verified with an oscilloscope. A reasonable delay is $\simeq$ 200 nsec, being the value measured at Yebes 180 nsec. The 10 MHz reference and the sampling clock (1024 MHz) were also detected and measured using a spectrum analyser.

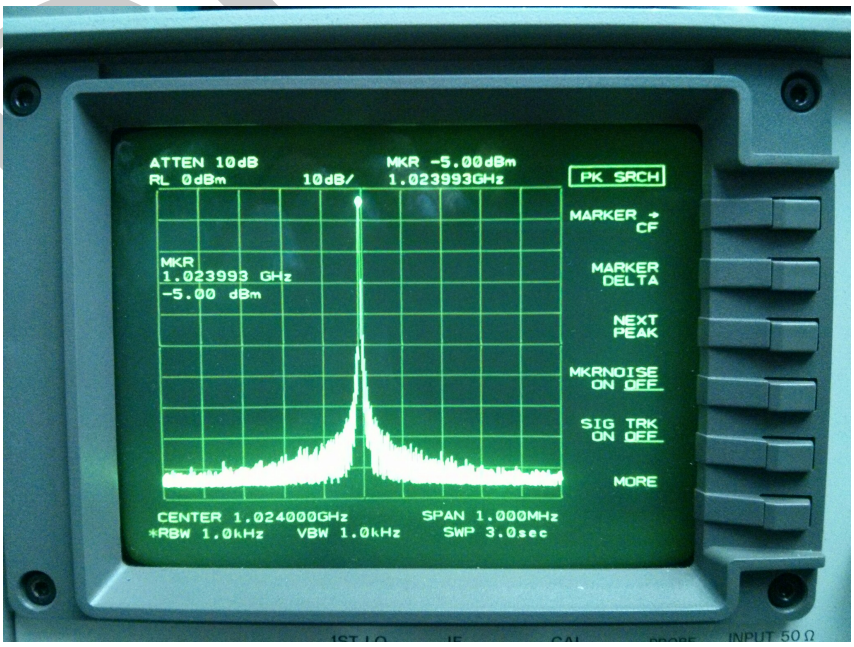


Figure 9: Sampling clock signal spectrum

Command `dbbcform = test, bin` implements an 8 bit-binary counter across all data

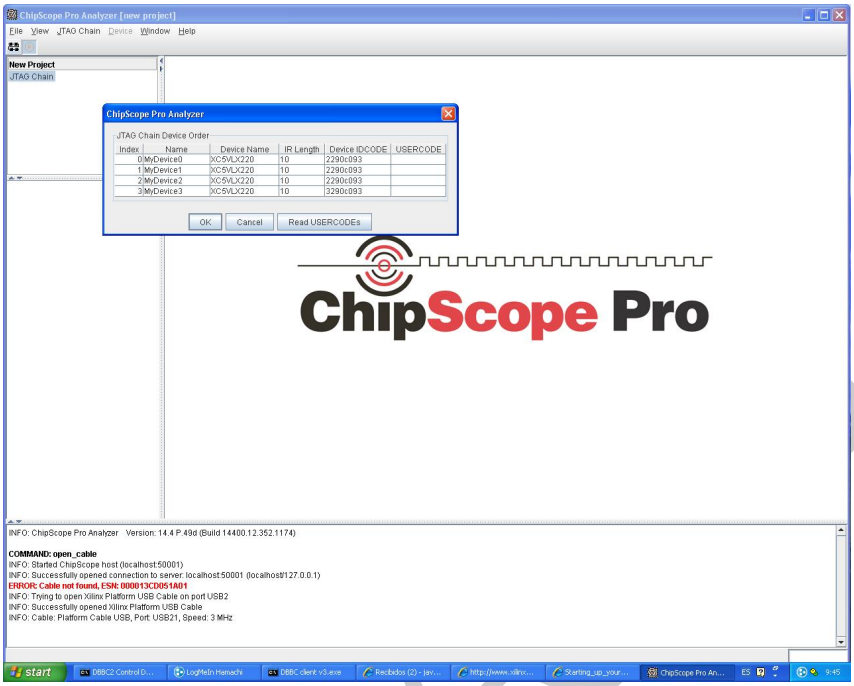


Figure 10: Detection of devices under the same USB-JTAG programmer.

lines (total of 8 counters). To diagnose the digital electronics performance, a software digital oscilloscope, aka Chipscope, is available at the DBBC embedded PC. Once the application is started, once should click on `open cable/search JTAG chain` to discover all the programmable devices under an specific USB port. Previously we selected the USB port we wanted to explore. Figure 10 shows an example of the four-cores DBBC digital stack detected by Chipscope at Yebes. Clicking the trigger button captures and displays one second of data flowing across the stack, which in this case must show the counter pattern. We found that in Yebes only two counters were successfully implemented within the first 16 lines of each Core2, while the remaining 48 lines contained noisy bits over the counter pattern (figure 11). Apparently this error was due to a mismatch between software versions and should not be considered relevant. LEDs 13 and 16 were not blinking synchronized.

Since LEDs 13 and 16 were not blinking synchronized, the DBBC was opened in a bench and inspected for loose connections. We found that a cable tie was stretching the flat cable used by the programmer, so the JTAG connector was not properly inserted. Removing the cable tie and resitting the JTAG apparently solved the synchronization problem.

G. Tuccari made a remote connexion to inspect the system but ended up with the conclusion that everything was behaving normal and those errors in the test pattern were due to incompatibilities between firmware and Chipscope version. Hat-Lab distributes a VPN software, that is already installed in the system, to perform remote assistance, called ”Hamachi”. Since it does not seem to work fine with Yebes (the connection is relayed), we installed temporarily ”Teamviewer”. Teamviewer generates a VPN with tunnelled traffic between the host and the server. Each server has an associated ID, and every session generates a new password. The client host connects to the VPN using this ID and the current password.

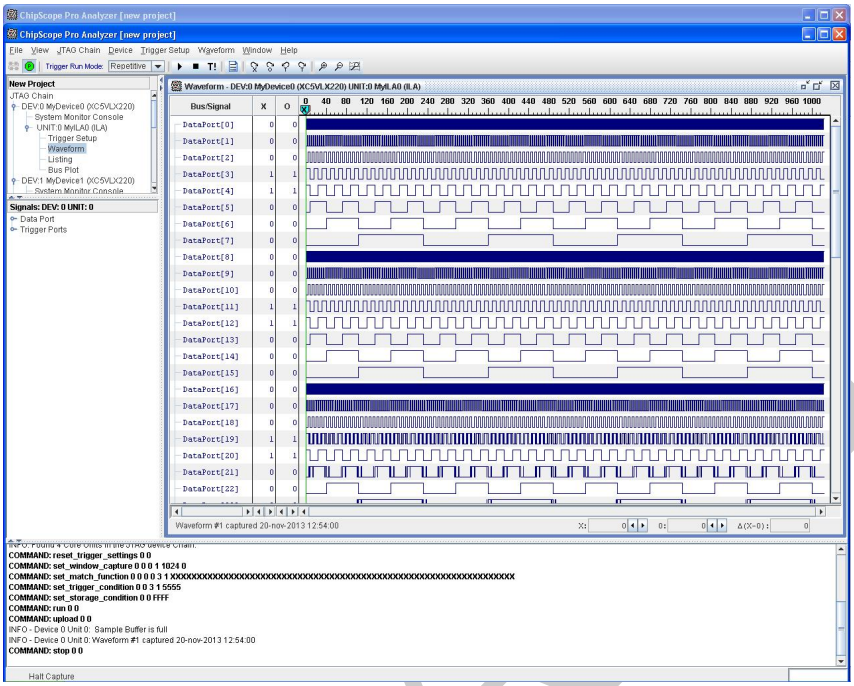


Figure 11: This screen capture shows two correct binary counters in the first 16 lines and another one wrong for the following 8 lines. Device 0 refers to the first core in the stack (IF A)

5 FiLa10G replacement

By the time the DBBC tests were performed, it arrived at Yebes a new FiLa10G card with two 10G ports that replaced the old one, which had a connectivity problem with one of the 10 Gb ports. The Fila10G is a standalone module which is close by the DBBC and connected to it via two VSI cables and a removable USB connection. The USB connection allows to load the firmware from the DBBC. Once it is loaded it is not required.

OMG3 Fiber optics with 10G connectivity goes from two XFP transceivers at the Fila 10G to the Harrobox to connect to the correlator via Internet and to the HP switch to connect to the Mark5C (more information in [4]). The Fila 10G has one serial and one ethernet port to allow for remote operations. However only one interface can be used at a time. Internally the Fila 10G does not have an ethernet card, but an ethernet to serial converter. By default the Fila 10G is internally cabled so that the serial port is connected. To enable the ethernet connection it is necessary to disconnect a cable and connect another one.

During the 4 Gbps demo in 2012 the FiLa10G was commanded using the serial port together with an external Lantronix serial-ethernet converter. Currently we are using the internal serial to ethernet converter which avoids using the external converter.

The Fila 10G can be controlled remotely through the ethernet port, but previous to that the firmware needs to be uploaded. This is achieved by plugging an USB port between it and the DBBC. An utility in the latter allows for this operation.

Three files are required to load the firmware: `FILA10GSA_load.bat` is the batch file that has to be run to setup the FILA10G-SA. This file makes use of other two, `FiLa10GSA_conf.cmd`

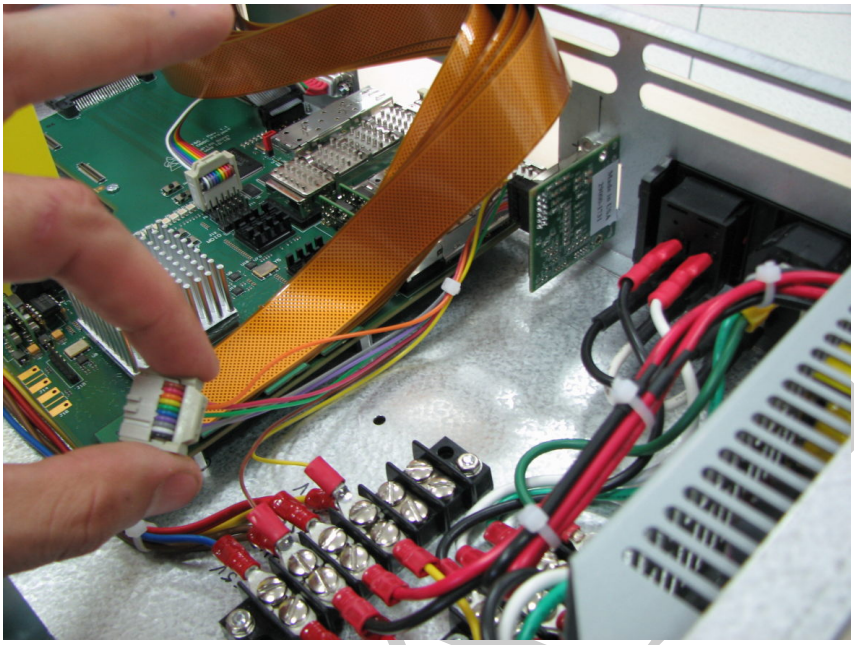


Figure 12: This picture shows the ethernet-to-serial converter inside FiLa10G unplugged from the board. Currently the internal converter is connected and hence the serial port is disabled.

that contains the set of instructions, and `fila10g_vX_Y_Z.bit` which is the firmware for the FILA10G-SA. The name of this latter file indicates the firmware version (X) and the type of FiLa10G in the system (Y). There are several versions of FiLa 10G's in the field with different FPGAs. At Yebes we use a stand-alone module with a Xilinx Virtex 4 inside (Xilinx xc4vfx60) and our Y parameter has to be equal to 1. Two iMPACT logs showing a failed and a successful programming can be found at Appendix 1.

Inside the DBBC and the Fila 10G there are two programmers connected to their USBs. Therefore, when the DBBC and the Fila 10G are connected through an USB cable, the system should be told which programmer should be used for each device. This is acomplished by modifying the ESN and port number in file "$C:\DBBC\bin\FiLa10GSA\_conf.cmd$" where the FiLa10G is connected. To know which port is the correct one, we ran the batch file "$C:\DBBC\bin\FILA10GSA\_load.bat$" and searched in the log for new ports when connecting/disconnecting the FiLa10G. The same result can be achieved using the Chipscope. There is another parameter in the commands file that might be modified showing the address of the device (-p). This value it's usually 1, but if there is no success one should try with 2, 3 ...

To command the FiLa10g-SA there are some python scripts in the FS computer under `/usr2/oper/bin` written by J. Wagner and Uwe Bach that use TCP/IP sockets to configure the module and allow the user to inject specific commands (see `DBBC2 FILA10G Command set v2_0.pdf` for a list of available commands).

6 Phase calibration

The manufacturer recommends to perform what is called a "phase calibration" after any hardware modification. This procedure was described in chapter 6 from [5]. Using three splitters and two attenuators (6 and 3 dB) the four cores were calibrated at a time. Values found for the calibration in DDC and PFB modes are:

Observing mode	IFa	IFb	IFc	IFd
DDCv104	216	221	227	81
PFBv14	79	207	79	90

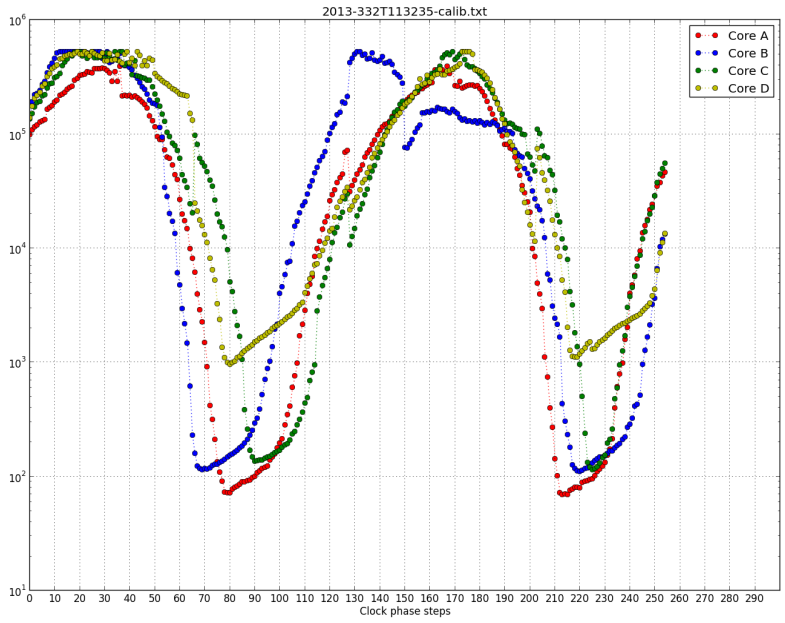


Figure 13: DDCv104 phase calibration data

7 Linearity study

A similar study to the one detailed in [6] about DBBC detectors linearity was performed after reinstallation, seeking for improvement specially in the base band detection. The main difference between both procedures was the agc setup, this time switched to man, 0, in order to introduce minimal degradation in SNR, and no monitoring with external detectors was used. Also a newer DDC mode version was used, DDCv104 instead of DDCv103.

Different axes with different scales were used to display data. The X axis is in dB, therefore it is a logarithmic scale. Total IF power is in a linear scale since its detection is logarithmic. The power detected for individual channels is in a logarithmic scale because the detection is linear.

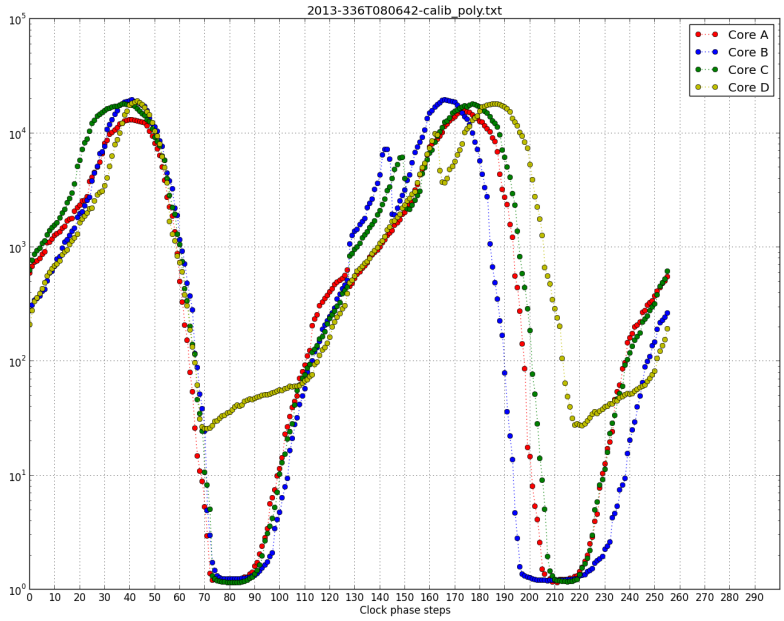


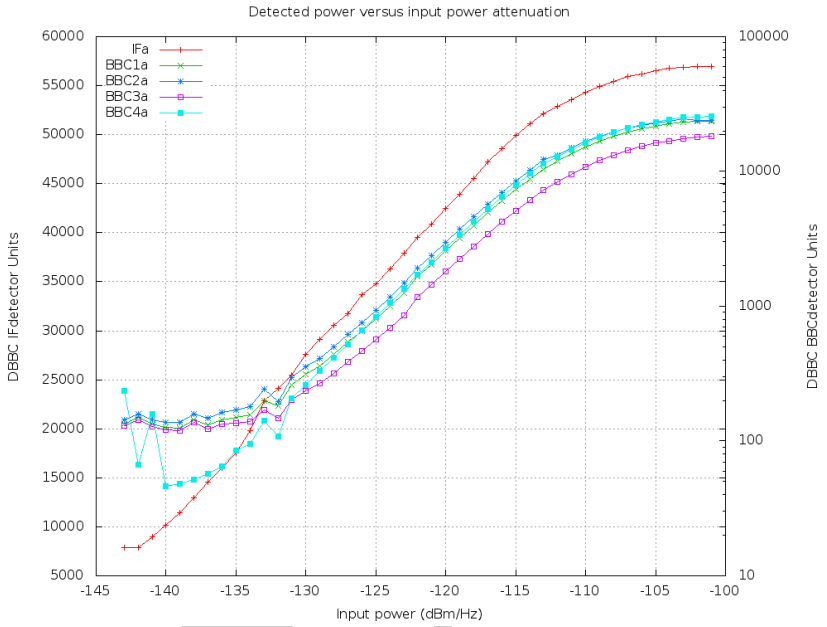
Figure 14: PFBv14 phase calibration data

These two scales allow to compare the linearity of both detections at a glance.The absolute power is displayed in the horizontal axis to have an easy reference for the arbitrary counts from the detectors.

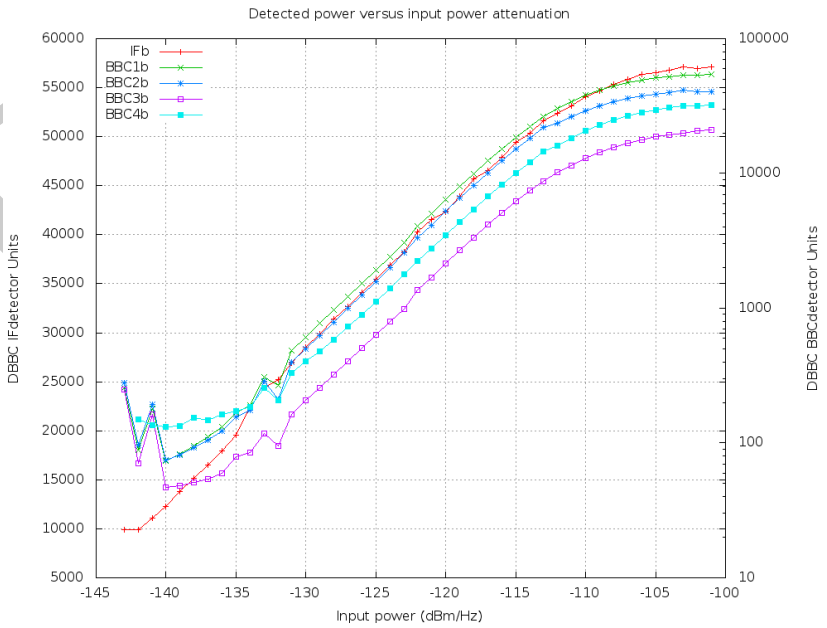
Relative to data in figure 15 from the DDC observing mode, the total IF power detection has not experimented any relevant improvement (as expected), but still has a large dynamic range that reaches saturation at about 50000 counts (30 dB of dynamic range), but surpisingly the SNR does not seem to have improved in any base band detector, moreover it is worse now for IFC and IFD than it was before the hardware modifications. Total IF power has to increase now over 43000 to allow BBCs to behave in a linear way while according to the results in [6] this threshold stood at 35000 before the updates. This experiment must be repeated to check repeatability of results, including the exchange of core2 position in the stack to discard position-dependency before investigating a problem of sensitivity in some of the cores.

In the other hand, these measurements show a little improvement when observing through PFB configuration with respect to the last test. Core2-A and Core2-C behave linearly from $\simeq$ 23000 to more than 50000, and for all channels. Core2-C has experimented a significant improvement since data from February were completely erratic. Core2-B and Core2-D have less linear range although still enough, starting at approximately 35000 IF counts until above 50000. There is a special issue involving Core2-D data. The first narrow bandwidth channels have different slopes. This maybe related with lack of power, as we have seen that the first channels in every Core-2 show less power than the rest. In any case special attention should be paid in the future to this Core-2 when running in PFB mode.

As with the first report, we have summarized the linearity intervals for the different modes

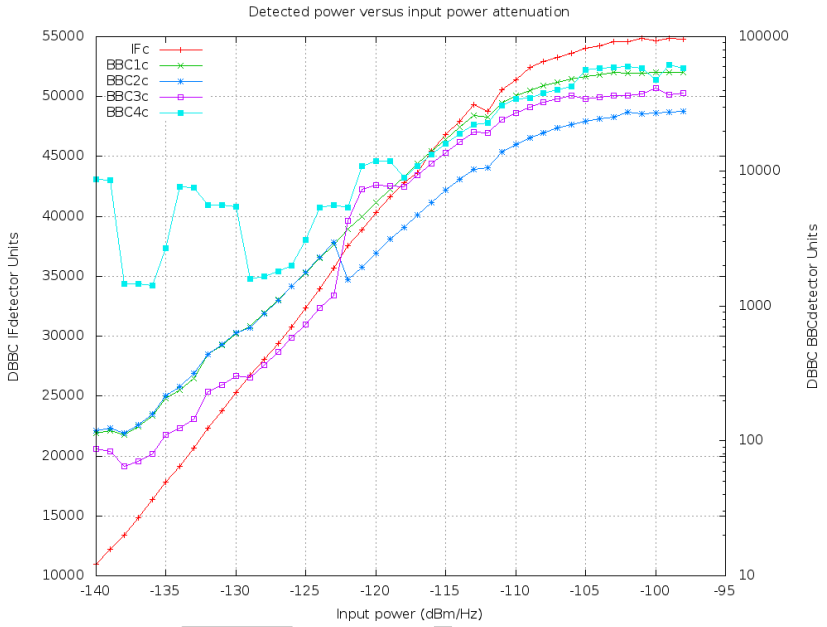


(a)

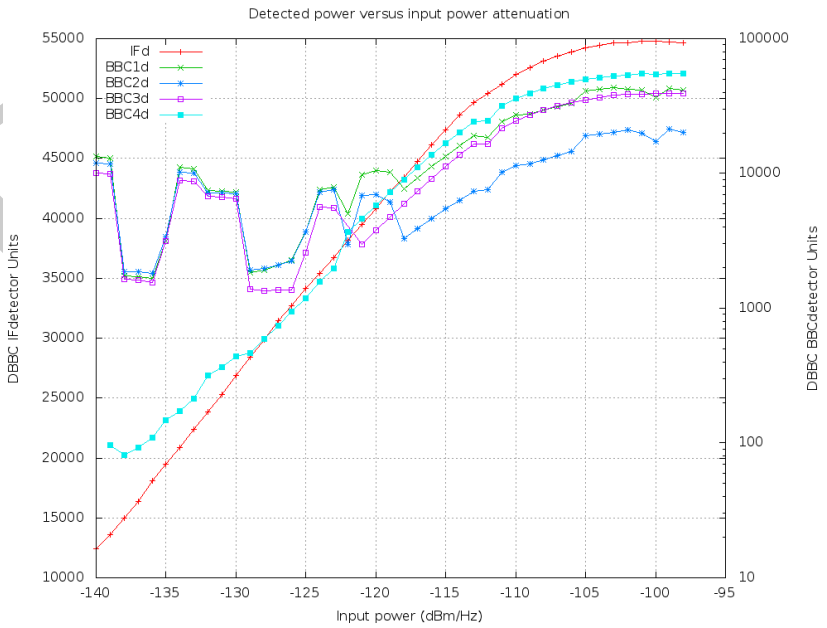


(b)

Figure 15: Power detection in the first two IFs and respective DDC channels.

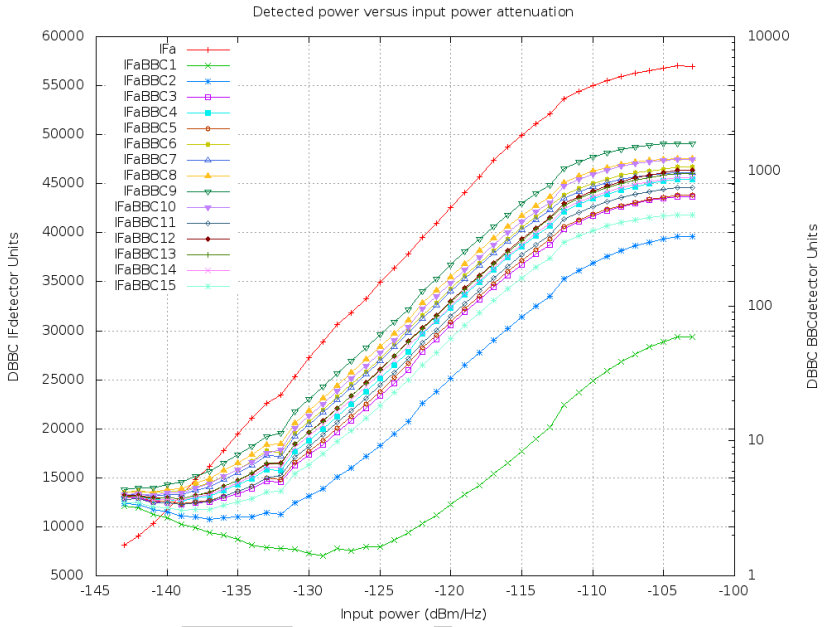


(c)

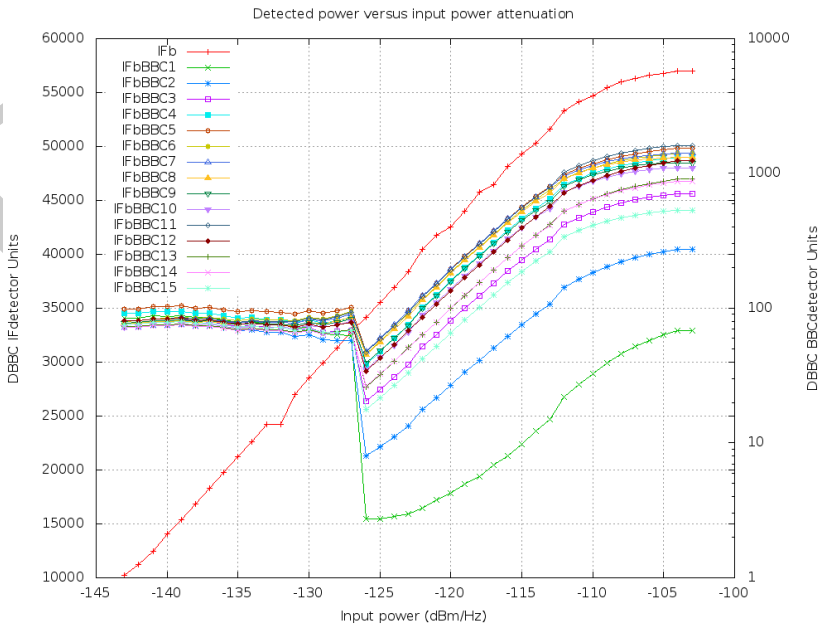


(d)

Figure 14: Power detection in the last two IFs and respective DDC channels.

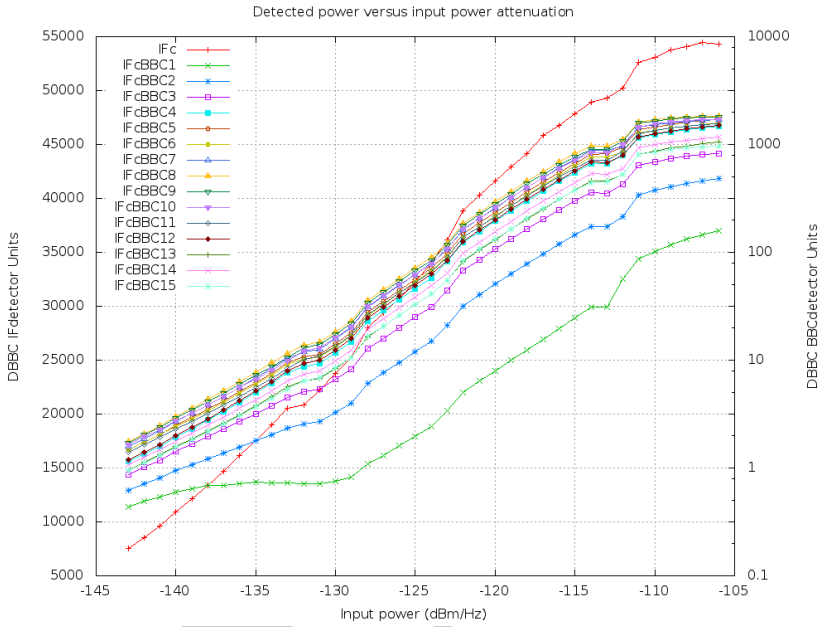


(a)

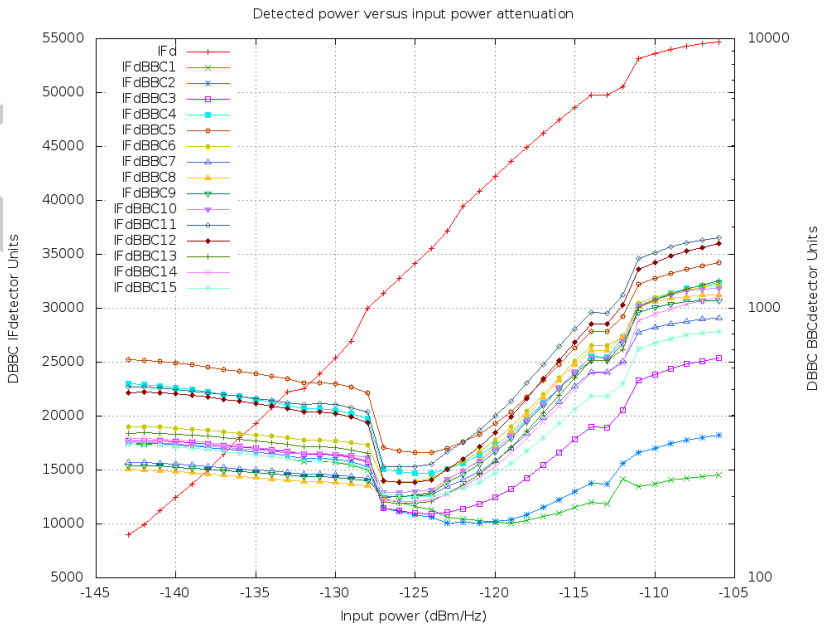


(b)

Figure 15: Power detection in the first two IFs and respective PFB channels.



(c)



(d)

Figure 14: Power detection in the last two IFs and respective PFB channels.

Power detector	DDC	PFB
IF A wide band	7500-50000	7500-50000
Core2 1 narrow band	25000-50000	35000-50000
IF B wide band	12000-50000	12000-50000
Core2 2 narrow band	25000-50000	38000-50000
IF C wide band	10000-50000	7500-50000
Core2 3 narrow band	42500-50000	25000-50000
IF D wide band	12500-50000	9000-50000
Core2 4 narrow band	42500-50000	38000-50000

Figure 15: Input power regimes, measured in counts, at which the power detection is linear. The narrow band detection is done in the COREs

and COREs in table 15.

In view of the results of this experiment we agree that detectors at both observing modes are ready for radiometry. However some of the items discussed above should be further investigated since the small linear interval for IFC and IFD runs the risk of saturating the detectors.

We would like to stress that:

- Base band channels AGC is gain, not attenuation as happens with conditioning modules.
- When a side band in a Core2 reaches saturation (65535) the other one automatically goes into saturation **even though it has different gain settings**.
- In DDC mode, when a base band channel is saturated one LED at the front panel lights identifying the channel, being the upper one related to channel 1, second related to channel 2 and so on.
- $dbbc = all, 20, 30$ sets **all** channels gain to the values given, upper side band and lower side band respectively.

8 R4616 IVS experiment and phasecal tones phase instability

On December 19th and 20th a 24h geodetic experiments was performed at Yebes running two backends system in parallel. While the analog system was commanded by the same FS that controlled the antenna, the DBBC was connected to its own dedicated FS and Mark5B+ to record data. This setup allows a debug of the digital system. The following e-mail includes the correlation results form the Washington correlator (WACO):

```
> YEBESDBC (Yd/A): Testing DBBC for YEBES40M.
>
>      Phasecal amplitudes in S-band channels SR1U,
>      SR2U, SR3U and SR4U tended to be low, leading to
>      'H' codes throughout.
>
```

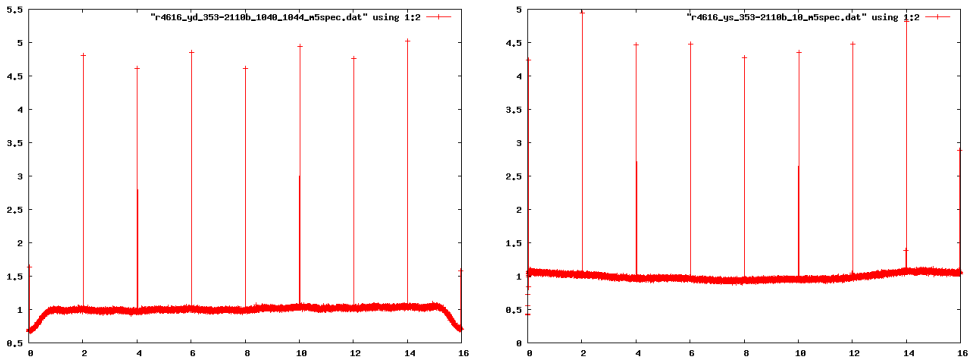
```
>      Phasecal in X-band is very noisy, such that any
>      manual phasecal chosen leads to low quality codes
>      on the rest.
>
>      Manual phasecal was applied at YEBESDBC in the
>      interest of exporting as much potentially useful
>      data as possible, but this had the effect of lowering
>      X-band data quality considerably, and leading to
>      closure problems.
>
>      Single-band delays in X-band oscillate every 2 hours
>      or so, on a scale of approximately 0.04 microseconds.
>
>      Low fringe amplitudes in channel SR4U throughout, and
>      low fringe amplitudes in all S-band channels at
>      various points during the experiment.  Tends to behave
>      in groups -- SR1U through SR3U will occasionally all
>      have low amplitudes while SR5U and SR6U are fine (the
>      other way around as well).
>
>      In X-band, low fringe amplitudes in XR1U/L generated
>      'G' codes.  Occasional low fringe amplitudes in XR3U
>      and XR4U as well.
>
>      Channels SR4U and XR1U/L removed from fringe fitting.
```

First basics diagnostics could be done at Yebes using some tools available at Mark5 (oper/bin) with the data recorded in the diskpacks. These software reads the mk5b file written by the `disk2file` command from `dimino` and make some sofisticated data processing that help with diagnosis of problems at the stations (They can also be found at `ftp://web.haystack.mit.edu/pub/mark5/B/util/`). 7 slots 4 seconds long were extracted from scan $30 : 353_2110b$.

- **m5spec.** Forms spectra of each sampled channel in a baseband data file. Was run as follows:
  ```
  m5spec -nopol r4616_ys_353-2110b_10.m5b Mark5B-512-16-1 4000
  10240 r4616_ys_353-2110b_10_m5spec.dat
  ```

  To understand what all the parameters and options mean just run m5spec with no arguments. Results are shown in figure 16, where a good SNR can be seen for both recordings. One strange behaviour that can be detected at a glance is that the base band channel spectrum in the vlba5 terminal does not roll off at the end of the band although it is expected that the base band filter drops the power 3 dB at 7.4 MHz. However, any wrong behaviour is detected for the dbbc spectrum at least for the first channel.

- **bpcal.** Calculates amplitude and phase of the phase cal tone given as argument for in each channel in the file.



(a) (b)

Figure 16: mk5spectra spectrum 4 seconds data recorded at 21:10:40 (bbc overlapped), scan r4616_ys_3532110b. a) DBBC, b) VLBA5

```
bpcal <input m5b filename> <tone freq (kHz)> [<#frames>]
```

In the 7 samples, 1 second of data recorded, and approximately 1 minute apart, time series for 16 bbcs and 2010 KHz tone, a phase instability can be easily appreciable for the digital backends, while the vlba5 terminal recordings does not change more than a few degrees. The first four channels are shown in figure 17 as example, while the same erroneous pattern was found for all bbc. Being this an important issue that can have impact on correlation, further tests were carried on to find out if the DBBC is modifying the phase of the signal.

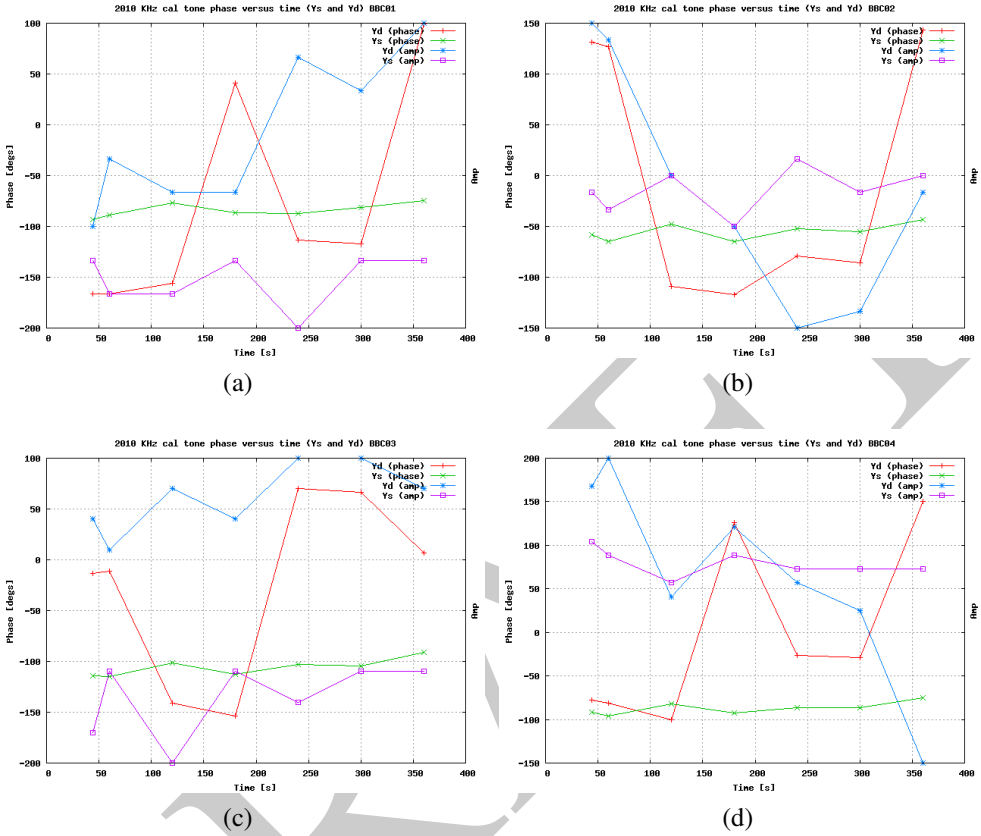


Figure 17: 2010 KHz pcal tone amplitude & phase for the first four channels within a r4616's scan. Extracted with bpcal

To get a better SNR and discard phase noise due to a third equipment between the analog terminal and the DBBC, a new cable setting was performed. Four splitters were installed at the patch panel so one copy from each IF signal went to the VLBA5 and the other one to the DBBC, instead of obtaining the copy for the DBBC from inside the VLBA5 terminal and going afterwards to the FFT preprocessor before injecting the signal to the DBBC. This should be the final setting of cables until the analog terminal ends it operations and the DBBC remains alone.

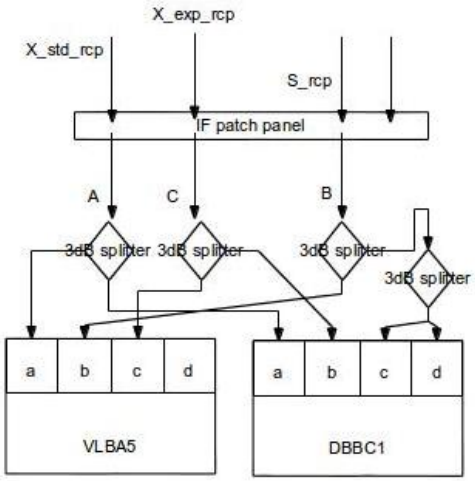


Figure 18: New IF cabling since January 2014

Phase cal tests at Yebes consisted on recording several minutes of data at X_std_RCP, X_exp_RCP and S_RCP band while phase cal is on and extracts pcal tones for every channel searching for phase instability. The procedure is described by de Vicente (2014) in report 2014-4.

Using the same setup as in r4616, pcal tones phase show stability for these minutes-scale tests in every Core2 except that corresponding to IFC (copy of S band), where tens of degree jumps can be easily detected (Figure 19c and 19d). To help with the interpretation of data a table showing the channel mapping for a typical geodesy experiment is included in the appendices section. Inside the DBBC each IF goes into an specific Core2, which can implement up to 4 bbc. Therefore, channels 1 to 4 belong to the first Core2, 5 to 8 to the second and so on. The last two channels from the last Core2 are not usually included in the observation. Notice that data from channels 1LSB and 8LSB are not valid since there is no tone at 2010 KHz for those channels (lower bands has pcal tones at $990 + n * 1000$ KHz)

Other tones (10 KHz, 1010 KHz, 3010 KHz...) showed similar unstabilities.

9 VSI-1pps drift

As suggested by G. Tuccari, an oscilloscope was connected to 1pps_out and 1pps_mon outputs at the back panel of DBBC to monitor time difference between the 1pps that feeds the DBBC (1pps_out) and the 1pps generated after the DSP that travels through the VSI cable (1pps_mon). A significant drift in a 24 hours period was discovered, therefore a time counter was configured with a PC to start a register of the delay between pulses every second. Below is the plot with the first 16 hours log (Figure 20).

The difference between pulses was increasing in a non-linear trend, which could be due to a mismatch in oscillation frequency. The evolution of the delay consists on discrete jumps that follows no clear pattern in time or amplitude but always in the positive direction following a sort of quadratic curve. With the experience that bad connexions usually results in synchronization

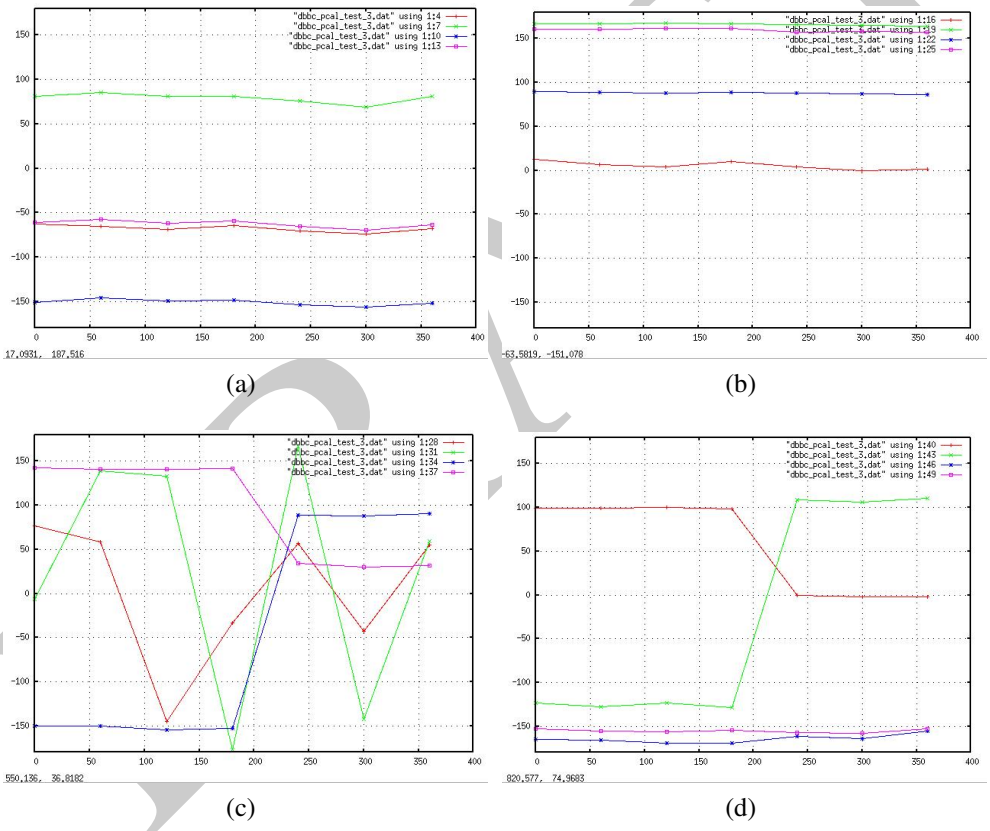


Figure 19: bpcal phase extractions for tone at 2010 KHz using the same configuration in r4616 a) 1USB, 2USB, 3USB, 4USB, b) 5USB, 6USB, 7USB, 8USB, c) 1LSB, 8LSB, 9USB, 10USB, d) 11USB, 12USB, 13USB, 14USB

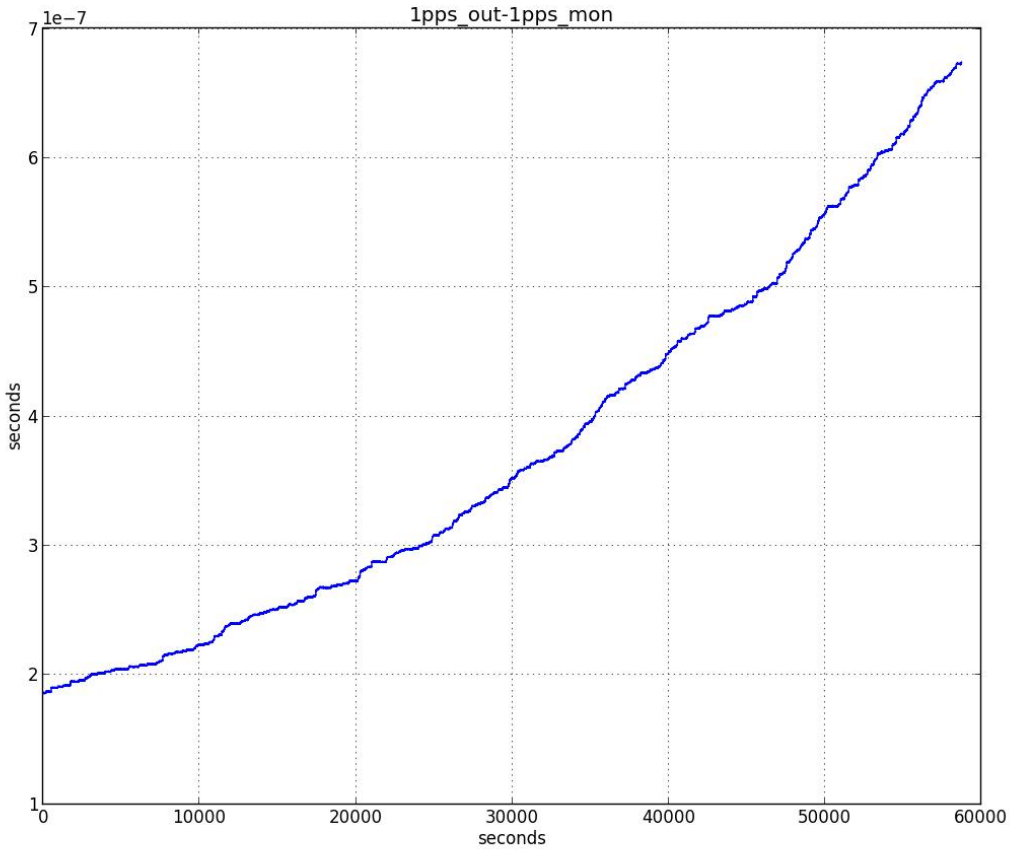


Figure 20: 1pps difference

problems (section 4.2), it was decided to disassembly the electronics, clean all the connectors with pressurized air and reassembly the system, with special care of not remaining any loose connection. After this operation the quadratic trend disappeared but 1 nsec jumps were still visible from time to time (figure 21).

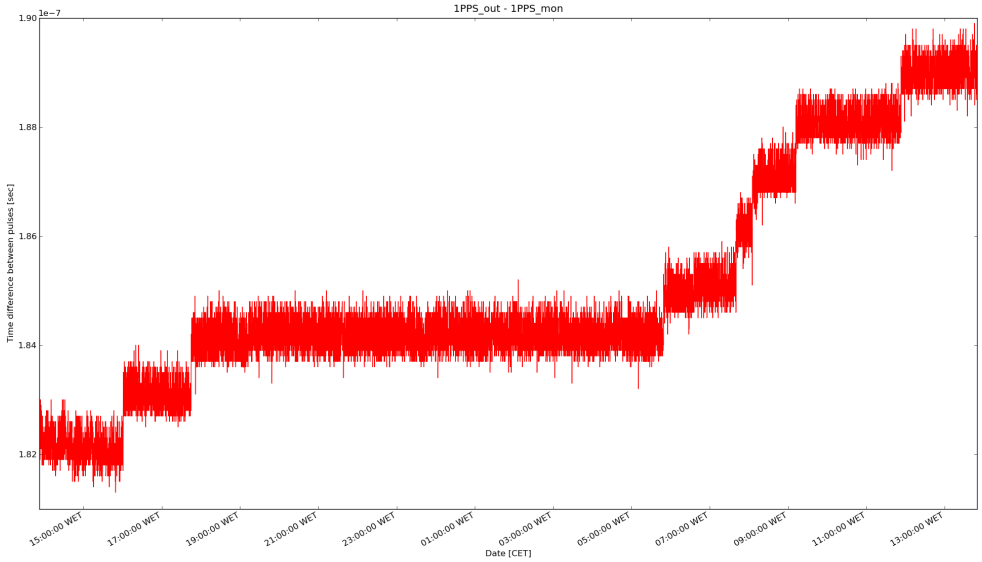


Figure 21: 1pps difference

To check the repercussion of last action in the phase stability of the pcal tones the test in previous section was repeated. Phase instability seemed to be solved when the first test was run, but when the test was performed a day later the jumps appeared again (figure 23 and figure 24).

With plots in figure 26, figure 23, figure 24, and the 1pps difference evolution for that time interval (figure 27) one can suspect that the jumps in the 1pps at VSI could be introducing instability in the phase of the pcal tones.

A wrench was used to tighten the connectors on hot trying to force jumps in the delay. To access the SMA connector that carries the clock signal in the ADB3 it is needed to bend the power supply cables for that same board. Just in that moment a new jump appeared at the oscilloscope. As other stations has reported problems with the cables, Yebes asked for another set of power cables to replace actual ones.

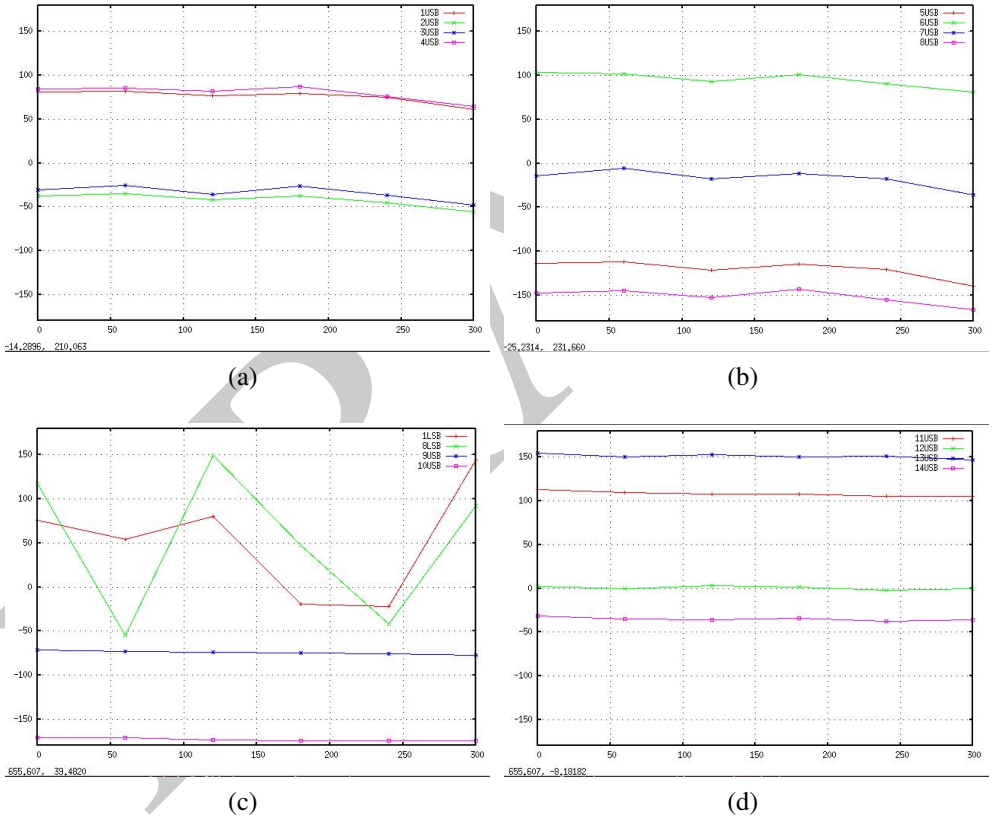


Figure 22: bpcal phase extractions for tone at 2010 KHz. Data recorded at 12:00:00 on 27/01/2014.

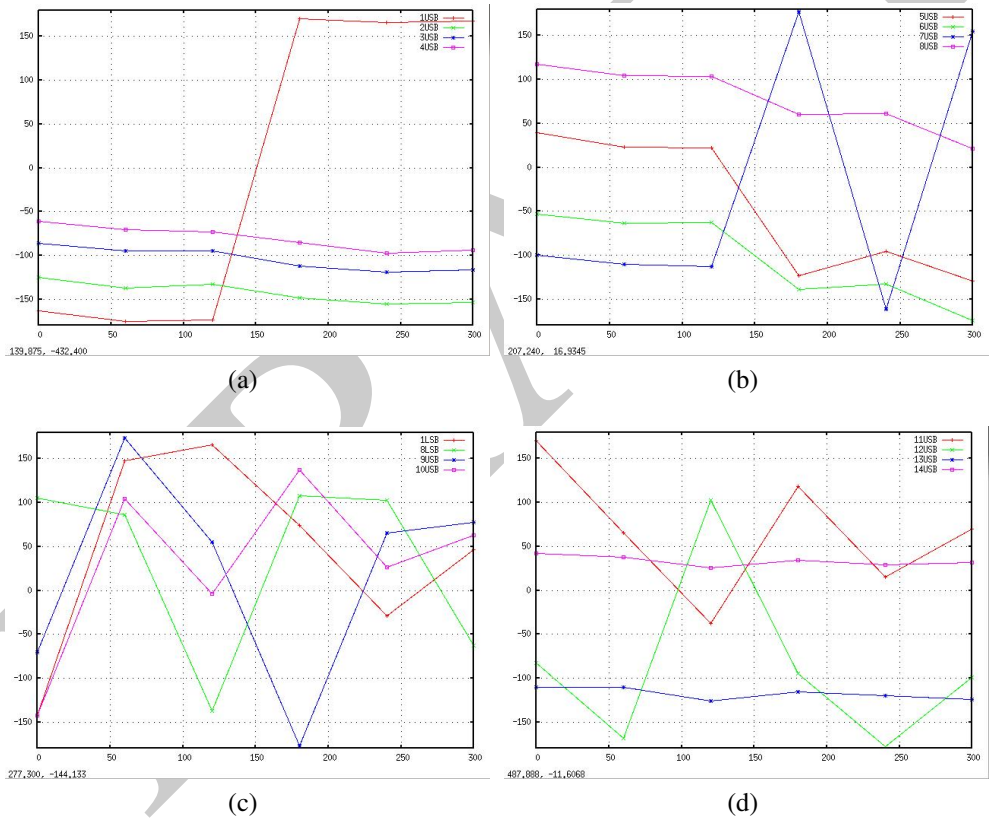


Figure 23: bpcal phase extractions for tone at 2010 KHz. Data recorded at 12:00:00 on 28/01/2014.

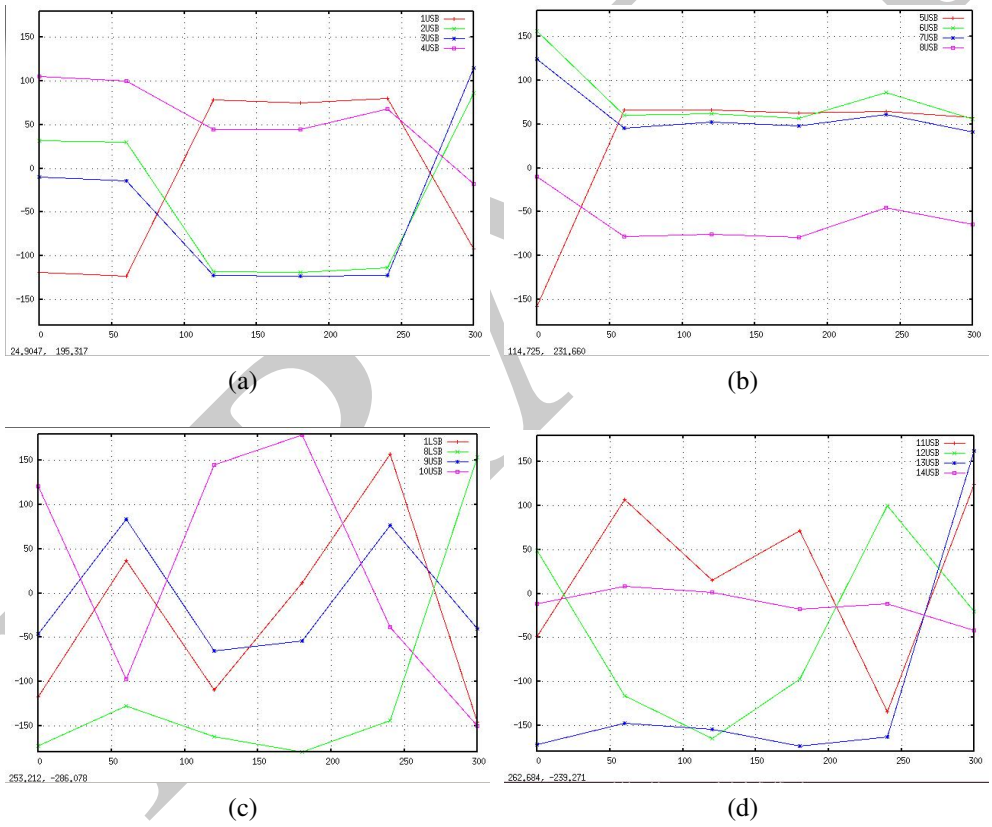


Figure 24: bpcal phase extractions for tone at 2010 KHz. Data recorded at 12:20:00 on 28/01/2014.

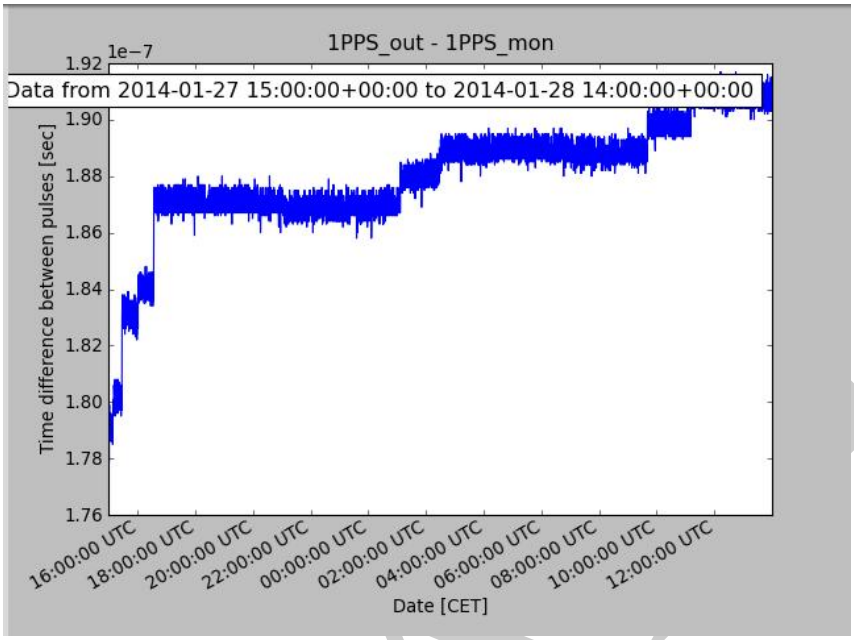


Figure 25: 1pps difference while experiment above

While waiting for the new set of replacement cables another IVS experiment was performed. This is a very brief correlation report for r4626:

```
> YEBDBBC  (Yd/C):  Testing DBBC for YEBES40M.
>
>    Phasecal signal is good in both bands, and fringe
>    amplitudes are very comparable to YEBES40M overall.
>
>    Small number of scans have low fringe amplitudes in
>    XR1U/L, leading to 'G' codes.
>
>    SBD in X-band looks good, but S-band has large rates
>    and breaks.  Over the course of ~4 hours, SBD decreases
>    by approximately 0.03 microseconds, resets to slightly
>    above the initial level, and repeats the process
>    trough the full experiment.
```

Once the cable replacement set arrived at Yebes, several tests done by P. de Vicente and A. Pérez using the new cables and swapping boards didn't solve the drift, raising the suspicious of a fundamental error in the system design. Some of the plots from these experiments are attached below.

During the following months several geodetic sessions with the same setup as the one described in section 8 showed the same phase unstability. More information about these experiments as well as a complete description of the full debugging procedure can be found in [7].

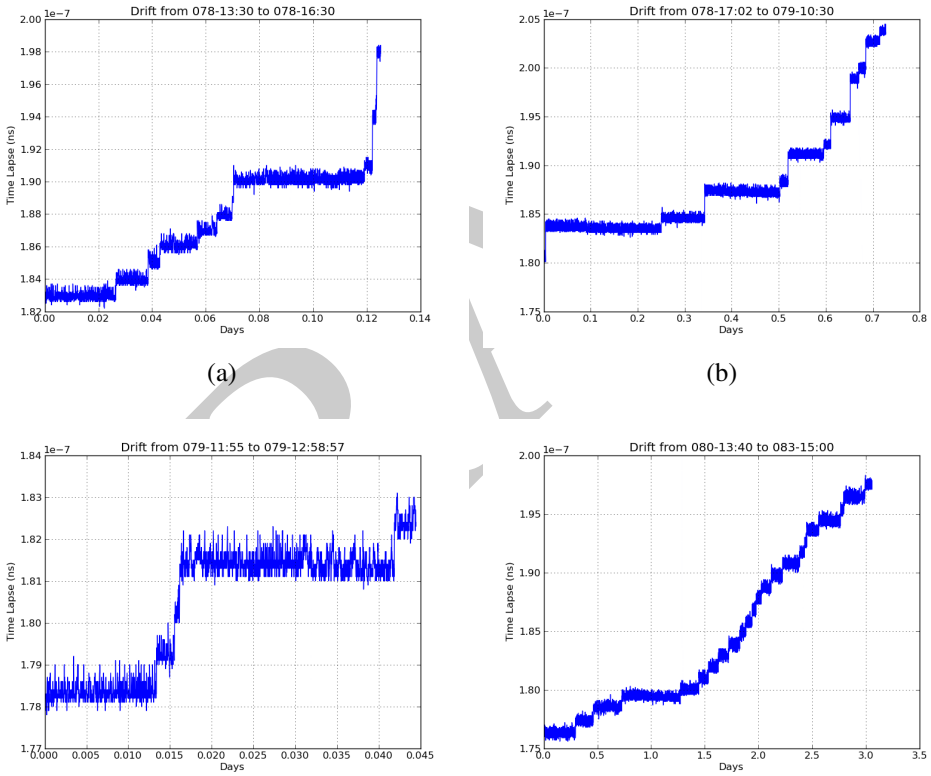


Figure 26: Several tests showing 1 pps drift. a) Swaped boards ADB1#3 and ADB1#4. b) CLK cable to ADB1#3 replaced by shorter one. c) ADB1#3 switched off. d) ADB1#3 and ADB1#4 switched off.

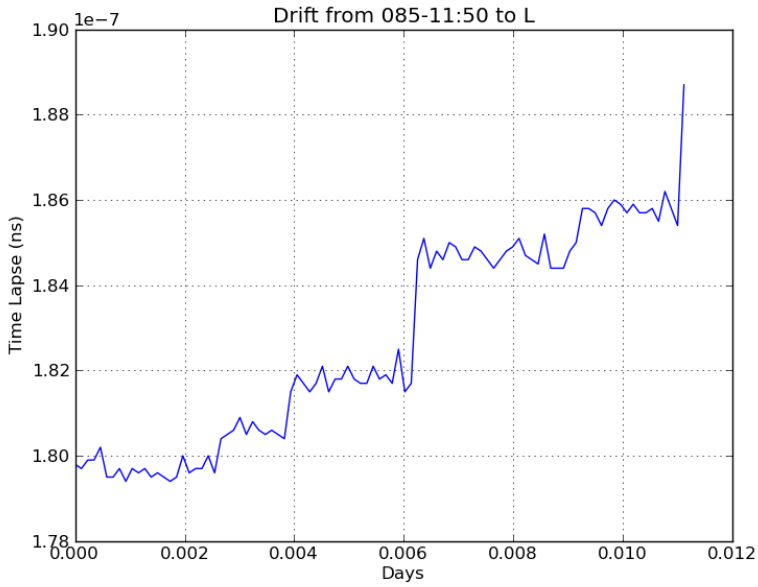


Figure 27: 1pps drift with a new ADB1#3 board.

10 Final modifications and tests

Finally in May 2014 the DBBC was sent back to MPIfR in Bonn for a final inspection. It was discovered that the power level from the power supplies at the last boards of the bus was marginal, furthermore below the nominal values. The voltage was adjusted and other minor modifications were performed like replacing the radiators at the COREs by narrower ones to avoid its proximity to the next ADB. After these modifications phase jumps disapperared, no 1 PPS drift was observed for days and stable fringes were found in X, Xband extended and S band for experiment R16xx.

Appendices

11 VSI channel mapping

MARK 4 SAMPLER TO VSI BIT STREAM MAPPING					
MARK 4 SAMPLER OUTPUT	VSI OUTPUT #1		MARK 4 SAMPLER OUTPUT	VSI OUTPUT #1 GEODETIC	VSI OUTPUT #2 ALL MODES
	VLBA	GEODETIC			
1US	0	0	9US	20	0
1UM	1	1	9UM	21	1
2US	2	2	10US	22	2
2UM	3	3	10UM	23	3
3US	4	4	11US	24	4
3UM	5	5	11UM	25	5
4US	6	6	12US	26	6
4UM	7	7	12UM	27	7
5US	8	8	13US	28	8
5UM	9	9	13UM	29	9
6US	10	10	14US	30	10
6UM	11	11	14UM	31	11
7US	12	12	15US		12
7UM	13	13	15UM		13
8US	14	14	16US		14
8UM	15	15	16UM		15
1LS	16	16	9LS		16
1LM	17	17	9LM		17
2LS	18		10LS		18
2LM	19		10LM		19
3LS	20		11LS		20
3LM	21		11LM		21
4LS	22		12LS		22
4LM	23		12LM		23
5LS	24		13LS		24
5LM	25		13LM		25
6LS	26		14LS		26
6LM	27		14LM		27
7LS	28		15LS		28
7LM	29		15LM		29
8LS	30	18	16LS		30
8LM	31	19	16LM		31
18-Dec-03			vsi4.xls		DAN SMYTHE

Figure 28: VSI channel mapping

12 Firmware load to FiLa10G aborted iMPACT log

```
C:\DBBC\bin>FILA10GSA_load.bat

C:\DBBC\bin>C:\Xilinx\12.4\LabTools\LabTools\bin\nt\impact
-batch FILA10GSA_conf
.cmd
Release 12.4 - iMPACT M.81d (nt)
Copyright (c) 1995-2010 Xilinx, Inc.  All rights reserved.
Preference Table
Name                  Setting
StartupClock          Auto_Correction
AutoSignature         False
KeepSVF               False
ConcurrentMode        False
UseHighz              False
ConfigOnFailure       Stop
UserLevel             Novice
MessageLevel          Detailed
svfUseTime            false
SpiByteSwap           Auto_Correction
AutoInfer             false
SvfPlayDisplayComments false
Enumerating cables. Please wait.
Connecting to cable (Usb Port - USB21).
Checking cable driver.
 Driver file xusb_xlp.sys found.
 Driver version: src=1029, dest=1029.
 Driver windrvr6.sys version = 10.2.1.0. WinDriver v10.21
 Jungo (c) 1997 - 2010
Build Date: Aug 31 2010 X86 32bit SYS
14:35:41, version = 1021.
=====================================================
Found cable - > ESN = 00001165F40F01.
=====================================================
Connecting to cable (Usb Port - USB22).
Checking cable driver.
 Driver file xusb_xlp.sys found.
 Driver version: src=1029, dest=1029.
 Driver windrvr6.sys version = 10.2.1.0. WinDriver v10.21
 Jungo (c) 1997 - 2010
Build Date: Aug 31 2010 X86 32bit SYS
14:35:41, version = 1021.
=====================================================
Found cable - > ESN = 00001615FB3F01.
=====================================================
Connecting to cable (Usb Port - USB23).
```

```
Checking cable driver.
 Driver file xusb_xlp.sys found.
 Driver version: src=1029, dest=1029.
 Driver windrvr6.sys version = 10.2.1.0. WinDriver v10.21
 Jungo (c) 1997 - 2010
Build Date: Aug 31 2010 X86 32bit SYS
14:35:41, version = 1021.
Connecting to cable (Usb Port - USB22).
Checking cable driver.
 Driver file xusb_xlp.sys found.
 Driver version: src=1029, dest=1029.
 Driver windrvr6.sys version = 10.2.1.0. WinDriver v10.21
 Jungo (c) 1997 - 2010
Build Date: Aug 31 2010 X86 32bit SYS
14:35:41, version = 1021.
 Cable PID = 0008.
 Max current requested during enumeration is 300 mA.
Type = 0x0005.
 Cable Type = 3, Revision = 0.
 Setting cable speed to 6 MHz.
Cable connection established.
Firmware version = 2401.
File version of C:/Xilinx/12.4/LabTools/LabTools/data/xusb_xp2.hex
= 2401.
Firmware hex file version = 2401.
PLD file version = 200Dh.
 PLD version = 200Dh.
Type = 0x0005.
ESN option: 00001615FB3F01.
Identifying chain contents...'0': : Manufacturer's ID = Xilinx xc4vfx60,
 Version
 : 8
INFO:iMPACT:1777 -
   Reading C:/Xilinx/12.4/LabTools/LabTools/virtex4/data/xc4vfx60.bsd...
INFO:iMPACT:501 - '1': Added Device xc4vfx60 successfully.
----------------------------------------------------------------------
----------------------------------------------------------------------
done.
Elapsed time =      1 sec.
Elapsed time =      0 sec.
Elapsed time =      0 sec.
Elapsed time =      0 sec.
'1': Loading file 'c:/DBBC_CONF/FilesDBBC/fila10g_v2_0.bit' ...
done.
INFO:iMPACT:1777 -
   Reading C:/Xilinx/12.4/LabTools/LabTools/virtex4/data/xc4vfx100.bsd...
INFO:iMPACT:501 - '1': Added Device xc4vfx100 successfully.
```

```
------------------------------------------------------------------------
------------------------------------------------------------------------
INFO:iMPACT:583 - '1': The idcode read from the device does not
match the idcode

   in the bsdl File.
INFO:iMPACT:1578 - '1':  Device IDCODE :
00000001111010110100000010010011

INFO:iMPACT:1579 - '1': Expected IDCODE:
00000001111011100100000010010011
Elapsed time =      0 sec.

C:\DBBC\bin>FILA10GSA_load.bat

C:\DBBC\bin>C:\Xilinx\12.4\LabTools\LabTools\bin\nt\impact
-batch FILA10GSA_conf
.cmd
Release 12.4 - iMPACT M.81d (nt)
Copyright (c) 1995-2010 Xilinx, Inc.  All rights reserved.
Preference Table
Name                 Setting
StartupClock         Auto_Correction
AutoSignature        False
KeepSVF              False
ConcurrentMode       False
UseHighz             False
ConfigOnFailure      Stop
UserLevel            Novice
MessageLevel         Detailed
svfUseTime           false
SpiByteSwap          Auto_Correction
AutoInfer            false
SvfPlayDisplayComments false
Enumerating cables. Please wait.
Connecting to cable (Usb Port - USB21).
Checking cable driver.
 Driver file xusb_xlp.sys found.
 Driver version: src=1029, dest=1029.
 Driver windrvr6.sys version = 10.2.1.0. WinDriver v10.21
 Jungo (c) 1997 - 2010
Build Date: Aug 31 2010 X86 32bit SYS
14:35:41, version = 1021.
=====================================================
Found cable - > ESN = 00001165F40F01.
=====================================================
Connecting to cable (Usb Port - USB22).
```

```
Checking cable driver.
 Driver file xusb_xlp.sys found.
 Driver version: src=1029, dest=1029.
 Driver windrvr6.sys version = 10.2.1.0. WinDriver v10.21
 Jungo (c) 1997 - 2010
Build Date: Aug 31 2010 X86 32bit SYS
14:35:41, version = 1021.
=====================================================
Found cable - > ESN = 00001615FB3F01.
=====================================================
Connecting to cable (Usb Port - USB23).
Checking cable driver.
 Driver file xusb_xlp.sys found.
 Driver version: src=1029, dest=1029.
 Driver windrvr6.sys version = 10.2.1.0. WinDriver v10.21
 Jungo (c) 1997 - 2010
Build Date: Aug 31 2010 X86 32bit SYS
14:35:41, version = 1021.
Connecting to cable (Usb Port - USB22).
Checking cable driver.
 Driver file xusb_xlp.sys found.
 Driver version: src=1029, dest=1029.
 Driver windrvr6.sys version = 10.2.1.0. WinDriver v10.21
 Jungo (c) 1997 - 2010
Build Date: Aug 31 2010 X86 32bit SYS
14:35:41, version = 1021.
 Cable PID = 0008.
 Max current requested during enumeration is 300 mA.
Type = 0x0005.
 Cable Type = 3, Revision = 0.
 Setting cable speed to 6 MHz.
Cable connection established.
Firmware version = 2401.
File version of C:/Xilinx/12.4/LabTools/LabTools/data/xusb_xp2.hex
= 2401.
Firmware hex file version = 2401.
PLD file version = 200Dh.
 PLD version = 200Dh.
Type = 0x0005.
ESN option: 00001615FB3F01.
Identifying chain contents...'0': : Manufacturer's ID = Xilinx xc4vfx60,
 Version
 : 8
INFO:iMPACT:1777 -
   Reading C:/Xilinx/12.4/LabTools/LabTools/virtex4/data/xc4vfx60.bsd...
INFO:iMPACT:501 - '1': Added Device xc4vfx60 successfully.
----------------------------------------------------------------------
```

```
----------------------------------------------------------------------
done.
Elapsed time =      1 sec.
Elapsed time =      0 sec.
Elapsed time =      0 sec.
Elapsed time =      0 sec.
'1': Loading file 'c:/DBBC_CONF/FilesDBBC/fila10g_v2_0.bit' ...
done.
INFO:iMPACT:1777 -
   Reading C:/Xilinx/12.4/LabTools/LabTools/virtex4/data/xc4vfx100.bsd...
INFO:iMPACT:501 - '1': Added Device xc4vfx100 successfully.
----------------------------------------------------------------------
----------------------------------------------------------------------
INFO:iMPACT:583 - '1': The idcode read from the device does not match the
idcode

   in the bsdl File.
INFO:iMPACT:1578 - '1':  Device IDCODE :
00000001111010110100000010010011

INFO:iMPACT:1579 - '1': Expected IDCODE:
00000001111011100100000010010011
Elapsed time =      0 sec.

C:\DBBC\bin>
```

13 Firmware load to FiLa10G successful iMPACT log

```
iMPACT Version: Nov 18 2010 22:01:18

iMPACT log file Started on Tue Feb 11 11:31:11 2014

Preference Table
Name                  Setting
StartupClock          Auto_Correction
AutoSignature         False
KeepSVF               False
ConcurrentMode        False
UseHighz              False
ConfigOnFailure       Stop
UserLevel             Novice
MessageLevel          Detailed
svfUseTime            false
SpiByteSwap           Auto_Correction
AutoInfer             false
SvfPlayDisplayComments false
```

```
Connecting to cable (Usb Port - USB21).
Checking cable driver.
 Driver file xusb_xlp.sys found.
 Driver version: src=1029, dest=1029.
 Driver windrvr6.sys version = 10.2.1.0. WinDriver v10.21
 Jungo (c) 1997 - 2010 Build Date: Aug 31 2010 X86 32bit SYS14:35:41,
  version = 1021.
 Cable PID = 0008.
 Max current requested during enumeration is 74 mA.
Type = 0x0004.
 Cable Type = 3, Revision = 0.
 Setting cable speed to 6 MHz.
Cable connection established.
Firmware version = 1029.
File version of C:/Xilinx/12.4/LabTools/LabTools/data/xusb_xlp.hex = 1303.
Firmware hex file version = 1303.
Downloading C:/Xilinx/12.4/LabTools/LabTools/data/xusb_xlp.hex.
Downloaded firmware version = 1303.
PLD file version = 0012h.
 PLD version = 0012h.
Type = 0x0004.
ESN option: 00001165F40F01.
Identifying chain contents...'0': : Manufacturer's ID = Xilinx xc5vlx220,
 Version : 3
INFO:iMPACT:1777 -
   Reading C:/Xilinx/12.4/LabTools/LabTools/virtex5/data/xc5vlx220.bsd...
INFO:iMPACT:501 - '1': Added Device xc5vlx220 successfully.
----------------------------------------------------------------------
----------------------------------------------------------------------
'1': : Manufacturer's ID = Xilinx xc5vlx220, Version : 2
INFO:iMPACT:501 - '1': Added Device xc5vlx220 successfully.
----------------------------------------------------------------------
----------------------------------------------------------------------
'2': : Manufacturer's ID = Xilinx xc5vlx220, Version : 2
INFO:iMPACT:501 - '1': Added Device xc5vlx220 successfully.
----------------------------------------------------------------------
----------------------------------------------------------------------
'3': : Manufacturer's ID = Xilinx xc5vlx220, Version : 2
INFO:iMPACT:501 - '1': Added Device xc5vlx220 successfully.
----------------------------------------------------------------------
----------------------------------------------------------------------
done.
Elapsed time =      1 sec.
Elapsed time =      0 sec.
Elapsed time =      0 sec.
Elapsed time =      0 sec.
'1': Loading file 'c:/DBBC_CONF/FilesDBBC/dbbc2_pfb_v14.bit' ...
```

```
done.
INFO:iMPACT:2257 - Startup Clock has been changed to 'JtagClk' in
 the bitstream   stored in memory,
   but the original bitstream file remains unchanged.
UserID read from the bitstream file = 0xFFFFFFFF.
----------------------------------------------------------------------
INFO:iMPACT:501 - '1': Added Device xc5vlx220 successfully.
----------------------------------------------------------------------
----------------------------------------------------------------------
'2': Loading file 'c:/DBBC_CONF/FilesDBBC/dbbc2_pfb_v14.bit' ...
done.
UserID read from the bitstream file = 0xFFFFFFFF.
----------------------------------------------------------------------
INFO:iMPACT:501 - '2': Added Device xc5vlx220 successfully.
----------------------------------------------------------------------
----------------------------------------------------------------------
'3': Loading file 'c:/DBBC_CONF/FilesDBBC/dbbc2_pfb_v14.bit' ...
done.
UserID read from the bitstream file = 0xFFFFFFFF.
----------------------------------------------------------------------
INFO:iMPACT:501 - '3': Added Device xc5vlx220 successfully.
----------------------------------------------------------------------
----------------------------------------------------------------------
'4': Loading file 'c:/DBBC_CONF/FilesDBBC/dbbc2_pfb_v14.bit' ...
done.
UserID read from the bitstream file = 0xFFFFFFFF.
----------------------------------------------------------------------
INFO:iMPACT:501 - '4': Added Device xc5vlx220 successfully.
----------------------------------------------------------------------
----------------------------------------------------------------------
Maximum TCK operating frequency for this device chain: 33000000.
Validating chain...
Boundary-scan chain validated successfully.
1: Device Temperature: Current Reading: -273.00 C
1: VCCINT Supply: Current Reading:   0.000 V
1: VCCAUX Supply: Current Reading:   0.000 V
2: Device Temperature: Current Reading: -273.00 C
2: VCCINT Supply: Current Reading:   0.000 V
2: VCCAUX Supply: Current Reading:   0.000 V
3: Device Temperature: Current Reading: -273.00 C
3: VCCINT Supply: Current Reading:   0.000 V
3: VCCAUX Supply: Current Reading:   0.000 V
4: Device Temperature: Current Reading: -273.00 C
4: VCCINT Supply: Current Reading:   0.000 V
4: VCCAUX Supply: Current Reading:   0.000 V
Elapsed time =      0 sec.
Maximum TCK operating frequency for this device chain: 33000000.
```

```
Validating chain...
Boundary-scan chain validated successfully.
1: Device Temperature: Current Reading: -273.00 C
1: VCCINT Supply: Current Reading:   0.000 V
1: VCCAUX Supply: Current Reading:   0.000 V
2: Device Temperature: Current Reading: -273.00 C
2: VCCINT Supply: Current Reading:   0.000 V
2: VCCAUX Supply: Current Reading:   0.000 V
3: Device Temperature: Current Reading: -273.00 C
3: VCCINT Supply: Current Reading:   0.000 V
3: VCCAUX Supply: Current Reading:   0.000 V
4: Device Temperature: Current Reading: -273.00 C
4: VCCINT Supply: Current Reading:   0.000 V
4: VCCAUX Supply: Current Reading:   0.000 V
Elapsed time =      0 sec.
Maximum TCK operating frequency for this device chain: 33000000.
Validating chain...
Boundary-scan chain validated successfully.
1: Device Temperature: Current Reading: -273.00 C
1: VCCINT Supply: Current Reading:   0.000 V
1: VCCAUX Supply: Current Reading:   0.000 V
2: Device Temperature: Current Reading: -273.00 C
2: VCCINT Supply: Current Reading:   0.000 V
2: VCCAUX Supply: Current Reading:   0.000 V
3: Device Temperature: Current Reading: -273.00 C
3: VCCINT Supply: Current Reading:   0.000 V
3: VCCAUX Supply: Current Reading:   0.000 V
4: Device Temperature: Current Reading: -273.00 C
4: VCCINT Supply: Current Reading:   0.000 V
4: VCCAUX Supply: Current Reading:   0.000 V
Elapsed time =      0 sec.
Maximum TCK operating frequency for this device chain: 33000000.
Validating chain...
Boundary-scan chain validated successfully.
1: Device Temperature: Current Reading: -273.00 C
1: VCCINT Supply: Current Reading:   0.000 V
1: VCCAUX Supply: Current Reading:   0.000 V
2: Device Temperature: Current Reading: -273.00 C
2: VCCINT Supply: Current Reading:   0.000 V
2: VCCAUX Supply: Current Reading:   0.000 V
3: Device Temperature: Current Reading: -273.00 C
3: VCCINT Supply: Current Reading:   0.000 V
3: VCCAUX Supply: Current Reading:   0.000 V
4: Device Temperature: Current Reading: -273.00 C
4: VCCINT Supply: Current Reading:   0.000 V
4: VCCAUX Supply: Current Reading:   0.000 V
Elapsed time =      0 sec.
```

```
Maximum TCK operating frequency for this device chain: 33000000.
Validating chain...
Boundary-scan chain validated successfully.
1: Device Temperature: Current Reading: -273.00 C
1: VCCINT Supply: Current Reading:   0.000 V
1: VCCAUX Supply: Current Reading:   0.000 V
2: Device Temperature: Current Reading: -273.00 C
2: VCCINT Supply: Current Reading:   0.000 V
2: VCCAUX Supply: Current Reading:   0.000 V
3: Device Temperature: Current Reading: -273.00 C
3: VCCINT Supply: Current Reading:   0.000 V
3: VCCAUX Supply: Current Reading:   0.000 V
4: Device Temperature: Current Reading: -273.00 C
4: VCCINT Supply: Current Reading:   0.000 V
4: VCCAUX Supply: Current Reading:   0.000 V
'1': Programming device...
 Match_cycle = NoWait.
Match cycle: NoWait
 LCK_cycle = NoWait.
LCK cycle: NoWait
done.
INFO:iMPACT:2219 - Status register values:
INFO:iMPACT - 0011 1111 1111 1110 0000 1011 1000 0000
INFO:iMPACT:579 - '1': Completed downloading bit file to device.
INFO:iMPACT:188 - '1': Programming completed successfully.
 Match_cycle = NoWait.
Match cycle: NoWait
 LCK_cycle = NoWait.
LCK cycle: NoWait
INFO:iMPACT - '1': Checking done pin....done.
'1': Programmed successfully.
Elapsed time =    16 sec.
Maximum TCK operating frequency for this device chain: 33000000.
Validating chain...
Boundary-scan chain validated successfully.
1: Device Temperature: Current Reading: -273.00 C
1: VCCINT Supply: Current Reading:   0.000 V
1: VCCAUX Supply: Current Reading:   0.000 V
2: Device Temperature: Current Reading: -273.00 C
2: VCCINT Supply: Current Reading:   0.000 V
2: VCCAUX Supply: Current Reading:   0.000 V
3: Device Temperature: Current Reading: -273.00 C
3: VCCINT Supply: Current Reading:   0.000 V
3: VCCAUX Supply: Current Reading:   0.000 V
4: Device Temperature: Current Reading: -273.00 C
4: VCCINT Supply: Current Reading:   0.000 V
4: VCCAUX Supply: Current Reading:   0.000 V
```

```
'2': Programming device...
 Match_cycle = NoWait.
Match cycle: NoWait
 LCK_cycle = NoWait.
LCK cycle: NoWait
done.
INFO:iMPACT:2219 - Status register values:
INFO:iMPACT - 0011 1111 1111 1110 0000 1011 1000 0000
INFO:iMPACT:579 - '2': Completed downloading bit file to device.
INFO:iMPACT:188 - '2': Programming completed successfully.
 Match_cycle = NoWait.
Match cycle: NoWait
 LCK_cycle = NoWait.
LCK cycle: NoWait
INFO:iMPACT - '2': Checking done pin....done.
'2': Programmed successfully.
Elapsed time =     17 sec.
Maximum TCK operating frequency for this device chain: 33000000.
Validating chain...
Boundary-scan chain validated successfully.
1: Device Temperature: Current Reading: -273.00 C
1: VCCINT Supply: Current Reading:   0.000 V
1: VCCAUX Supply: Current Reading:   0.000 V
2: Device Temperature: Current Reading: -273.00 C
2: VCCINT Supply: Current Reading:   0.000 V
2: VCCAUX Supply: Current Reading:   0.000 V
3: Device Temperature: Current Reading: -273.00 C
3: VCCINT Supply: Current Reading:   0.000 V
3: VCCAUX Supply: Current Reading:   0.000 V
4: Device Temperature: Current Reading: -273.00 C
4: VCCINT Supply: Current Reading:   0.000 V
4: VCCAUX Supply: Current Reading:   0.000 V
'3': Programming device...
 Match_cycle = NoWait.
Match cycle: NoWait
 LCK_cycle = NoWait.
LCK cycle: NoWait
done.
INFO:iMPACT:2219 - Status register values:
INFO:iMPACT - 0011 1111 1111 1110 0000 1011 1000 0000
INFO:iMPACT:579 - '3': Completed downloading bit file to device.
INFO:iMPACT:188 - '3': Programming completed successfully.
 Match_cycle = NoWait.
Match cycle: NoWait
 LCK_cycle = NoWait.
LCK cycle: NoWait
INFO:iMPACT - '3': Checking done pin....done.
```

```
'3': Programmed successfully.
Elapsed time =     16 sec.
Maximum TCK operating frequency for this device chain: 33000000.
Validating chain...
Boundary-scan chain validated successfully.
1: Device Temperature: Current Reading: -273.00 C
1: VCCINT Supply: Current Reading:   0.000 V
1: VCCAUX Supply: Current Reading:   0.000 V
2: Device Temperature: Current Reading: -273.00 C
2: VCCINT Supply: Current Reading:   0.000 V
2: VCCAUX Supply: Current Reading:   0.000 V
3: Device Temperature: Current Reading: -273.00 C
3: VCCINT Supply: Current Reading:   0.000 V
3: VCCAUX Supply: Current Reading:   0.000 V
4: Device Temperature: Current Reading: -273.00 C
4: VCCINT Supply: Current Reading:   0.000 V
4: VCCAUX Supply: Current Reading:   0.000 V
'4': Programming device...
 Match_cycle = NoWait.
Match cycle: NoWait
 LCK_cycle = NoWait.
LCK cycle: NoWait
done.
INFO:iMPACT:2219 - Status register values:
INFO:iMPACT - 0011 1111 1111 1110 0000 1011 1000 0000
INFO:iMPACT:579 - '4': Completed downloading bit file to device.
INFO:iMPACT:188 - '4': Programming completed successfully.
 Match_cycle = NoWait.
Match cycle: NoWait
 LCK_cycle = NoWait.
LCK cycle: NoWait
INFO:iMPACT - '4': Checking done pin....done.
'4': Programmed successfully.
Elapsed time =     17 sec.
----------------------------------------------------------------------
----------------------------------------------------------------------
----------------------------------------------------------------------
----------------------------------------------------------------------
----------------------------------------------------------------------
----------------------------------------------------------------------
```

References

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