Radiometry with the DBBC

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Revision history

Version	Date	Author	Updates
1.0	25-03-2012	P. de Vicente/J. González	First draft

Contents

1 Introduction

The goal of this report is to study the performance of radiometry with the DBBC using its two personality modes: DDC (Direct Down Conversion) and PFB (Polyphase Filter Bank) with the latest firmware versions available. We have used wide band and narrow band channels.

2 Hardware description

The DBBC at Yebes is currently (april 2013) connected to the VLBA IF data acquisition rack and to the FFT preprocessor as described in Fig. 1. This setup allows to detect the signal from the IF of any receiver simultaneously at the VLBA and DBBC and to monitor the signal in the first Nyquist zone in the FFTS in case of need just by exchanging a connector

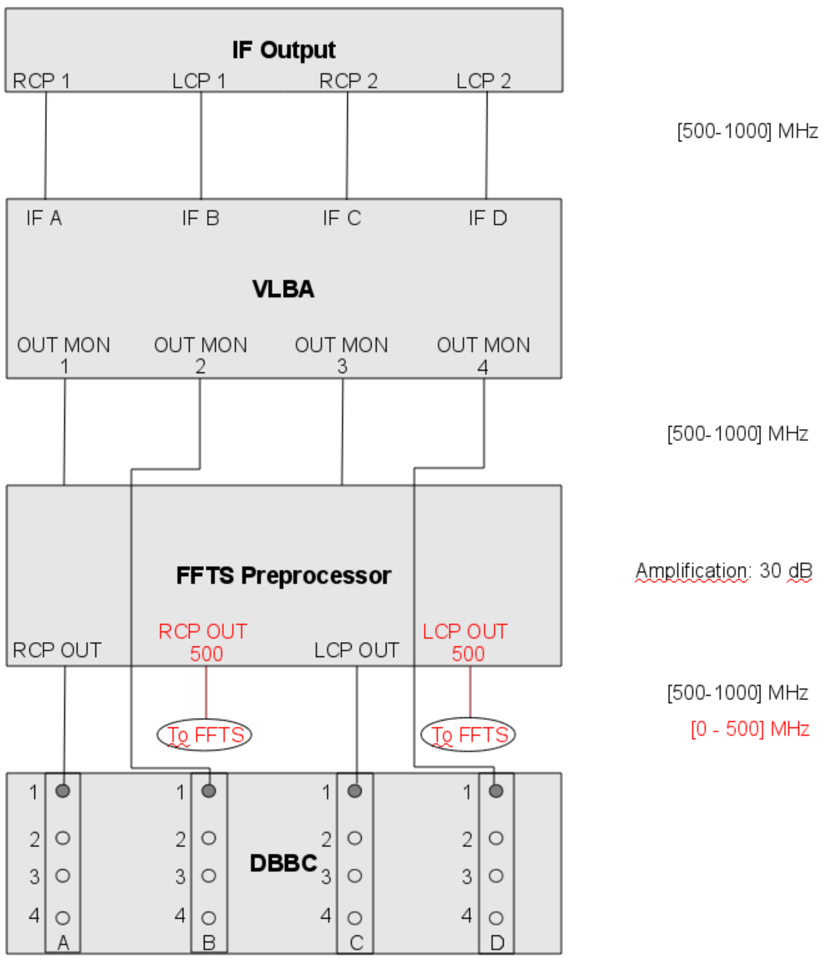

Figure 1: *Current IF - DBBC setup*

The DBBC has 4 independent modules, called CoMos (Conditioning Modules) that allow to work with 4 IFs (for example 2 pols and 2 IFs per pol) simultaneously. Each module has

4 SMA inputs which provide flexibility to use different setups avoiding to move cables from one connector to another. Each module only processes the signal from one connector at a time. Input connectors are selected using an internal switch and software commands.

The first stage of each CoMo is filtering. Our CoMos only have two filters: 10-512 MHz and 512-1024 MHz. As shown in Fig. 1 we usually use filter 2 (Nyquist zone 2), although in case of need we could use the first Nyquist zone using the FFTS preprocessor outputs that feed the FFTS.

After the filters, there is a gain control which allows to produce a constant output power for the next module in the chain (ADB boards). The attenuator can be controlled automatically or manually in steps of 0.5 dB between 32 dB and 1 dB, which for the user corresponds to values between 1 and 64 arbitrary units respectively. The power detection is done afterwards by an integrated circuit (Hittie HMC610LP4) which generates a continuum signal whose voltage is proportional to the power in the band and ranges from -2.45 V to 2.45 V. The detection is logarithmic. The working input power ranges from -48 dBm to -3 dBm which after being digitized with 16 bits, is converted to arbitrary units between 500 and 64000. The signal is read outside the board where the automatic gain control is computed for an optimum power level for the ADB modules. The required attenuation is sent back to the CoMo and applied before the IF output.

Fig. 2 shows a picture of an Unica2 CoMo board with labels that identify the two filters and the detecting power circuit. Two 3 dB splitters are also visible, although not tagged. The connectors on the right (TP out and IF out) are used internally to send the signals to other modules. The gain control is not visible in the board and we guess it is between the switch at the output of the filters and the first 3 dB splitter. The IF signal, once its level is adjusted to the optimum level, is sent via the ”IF out” connector to the ADB module.

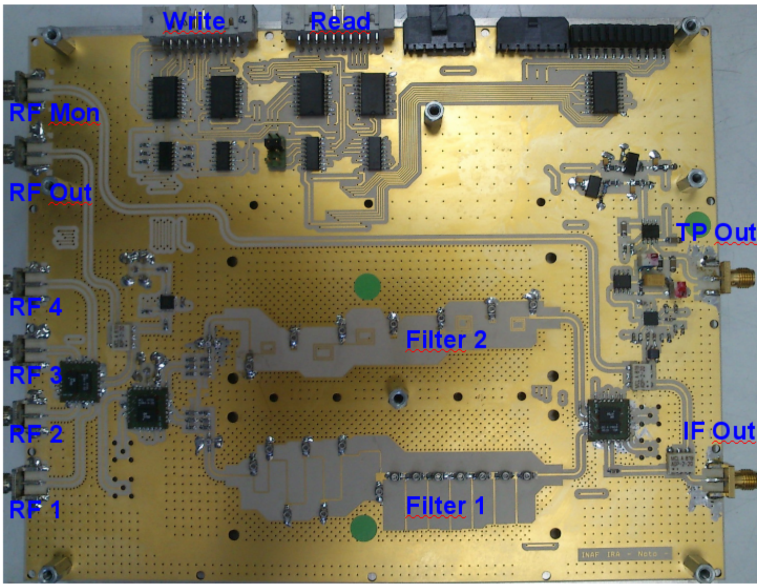

Figure 2: *CoMo board (Unica 2 version). The detection power circuit is in the upper right corner of the board (to the left of the green dot sticker)*

Fig. 3 shows the power read by the HMC610LP4 circuit as a function of the input power.

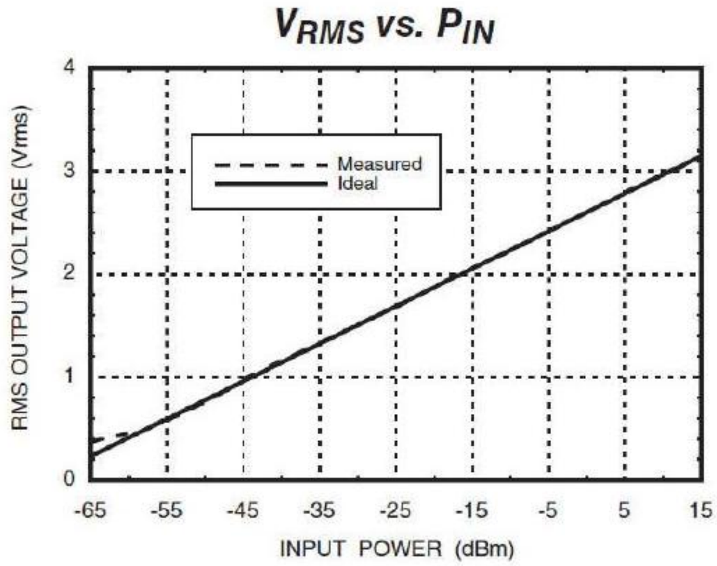

Figure 3: *Voltage power detected by circuit HMC610LP4 in the band as a function of the input power*

Two SMA connectors labeled “RF Mon” and “RF Out” are available in each CoMo. “RF Out” is a copy of the selected input in the module, “RF Mon” is a copy of the signal that goes to the ADB (Analog to Digital Board) with a power 3 dB lower. This difference arises from the two divisions: the first one is due to the monitoring and the second one to the voltage detection. The monitored signal has been filtered and its power level adjusted according to the automatic or manual gain control.

The signals from the CoMos are sent to the next module, the analog to digital boards, of which two version are currently available, ADB1 and ADB2. The DBBC at Yebes uses version 1. Every CoMo is connected to its ADB1 where the signal is digitized with 8 bits. Every board (in a stack together with the CORE boards and visible behind the front plastic cover) has 4 SMA connectors: 2 on the top for the IF and the clock, and 2 for a RESET signal from the Timing set board, which can be single-ended or differential. This signal is used to synchronize all boards in the stack. Since the RESET signal is single ended the free connector requires a 50 ohm load. Fig. 4 shows a picture of one of the AD boards after being removed from the stack.

Power for individual channels is detected from the 8 bit digitized signal at the FPGA in the CORE boards. The signal to be measured is extracted from the main flow and therefore any operation related to power mesurement, like auto gain control, performed in the COREs has no influence in the flow of the signal that is being recorded. For example, DDC mode version 103 allows to set to AGC or manual mode individual channels, but none of these operations modifies the amplitude of the signal that goes through the VSI bus.

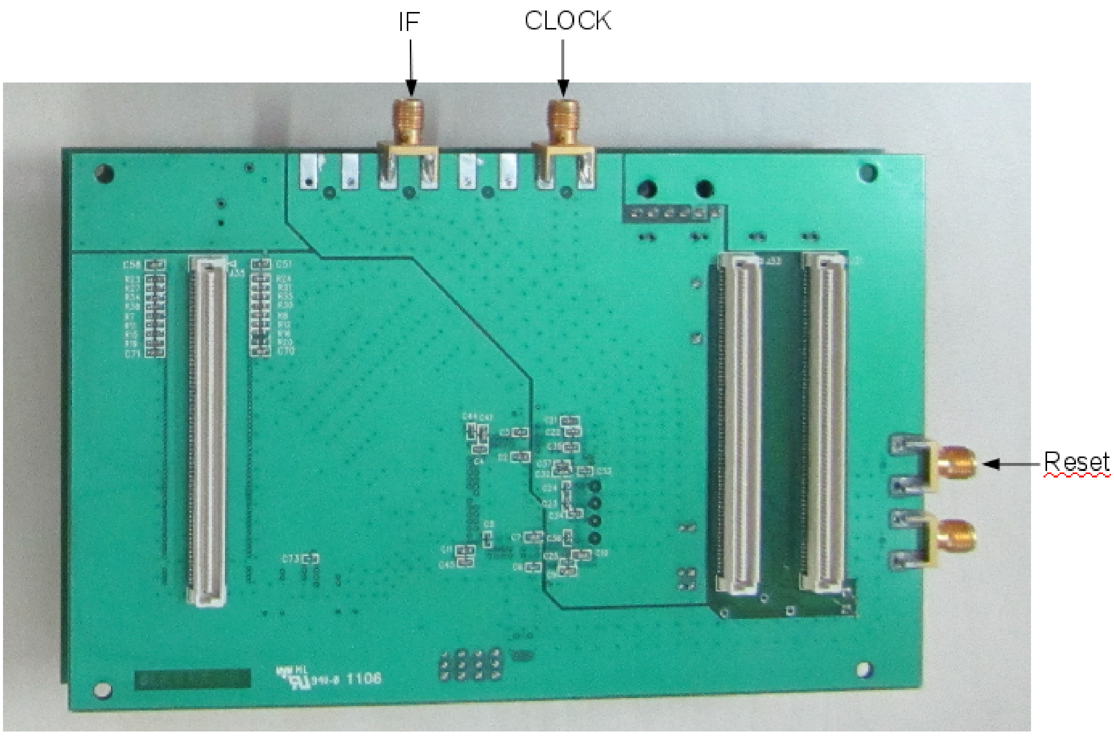

Figure 4: *ADB1 board with input connectors annotated*

3 Firmware versions

The control of the DBBC is done using software downloadable from HAT-Lab web page, where the firmware is updated from time to time. At Yebes we have tested version 102 and 103 for the DDC personality and version 14 for the PFB one. The number and structure of the commands may change between versions and all measurements should be taken with care taking into account this behaviour.

4 Prior to calibration: phase calibration

To obtain an optimum performance for the DBBC, phase calibration is required, both for the DDC (Direct Down Conversion) personality and the PFB (Polyphase Filter Bank). Phase calibration was done in DDC mode long time ago and the procedure and results were described by de Vicente et al. 2011. Basically it consists on injecting a -15dBm signal at 764 MHz in one input of the four CoMos and run command “calibration”from the client. Results are produced in 5 columns, the first containing the clock phase and the other 4 the results of the measurement for each CoMo. It is advisable to use several power splitters to measure all CoMos simultaneaously. The results from the calibration in PFB mode on March 13th 2013 are displayed in Fig. 5. The clock phase is determined by obtaining the value at which the minimum is achieved. Table 1 summarizes the final values.

As Fig. 5 shows, the minimum of the curves is less deep as we move along the stack. That

IF	min	phase
A	13	94
B	52	89
C	96	79
D	1474	192

Table 1: *Phases for each CoMo*

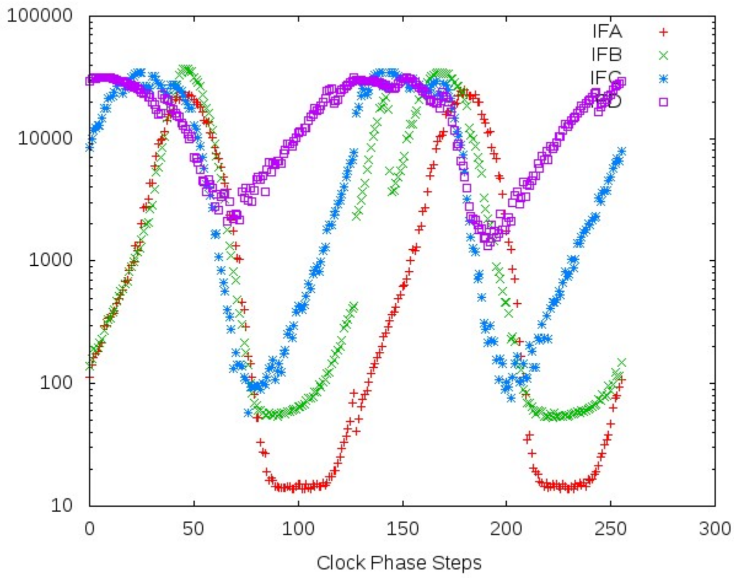

Figure 5: *Results from phase calibration. The optimum value for each IF was chosen for the minimum value. Since the dynamic range is quite large a logarithmic scale was used. The chosen values were 94, 89, 79 and 192 for IFs A, B, C and D respectively.*

is the minimum is more evident for IF A than for IF D. This behaviour might come from a loss of SNR as the signal travels along the stack. Further investigation should be performed to check it.

5 Measuring the linearity of the power detection

Measurements were done injecting white noise in a band between 100 MHz and 1100 MHz from a noise source generator into the IFs. The noise generator delivers -47 dBm/MHz and allows to control its power output using a 1 dB step attenuator, ranging from 0 to 50 dB. We measured two CoMos at a time using a 2 way splitter (Mini-Circuits ZFSC-2-11-S) with an operating frequency range between 10 and 2000 MHz. The output was measured using the Field System and in parallel we injected the "RF Mon" signal into a continuum detector (OAY-14) which works in the 50 to 1500 MHz frequency range. The continuum detector produces a continuum signal proportional to the detected power and it is read by a digital multimeter (Keithley 2701) using an integration time of 1 second. The IF attenuation in the CoMos was set to manual at a position of 20 which corresponds to 10 dB. These measurements were done both in DDC (firmware version 103) and PFB mode (firmware version 14) and are displayed in Fig. 6.

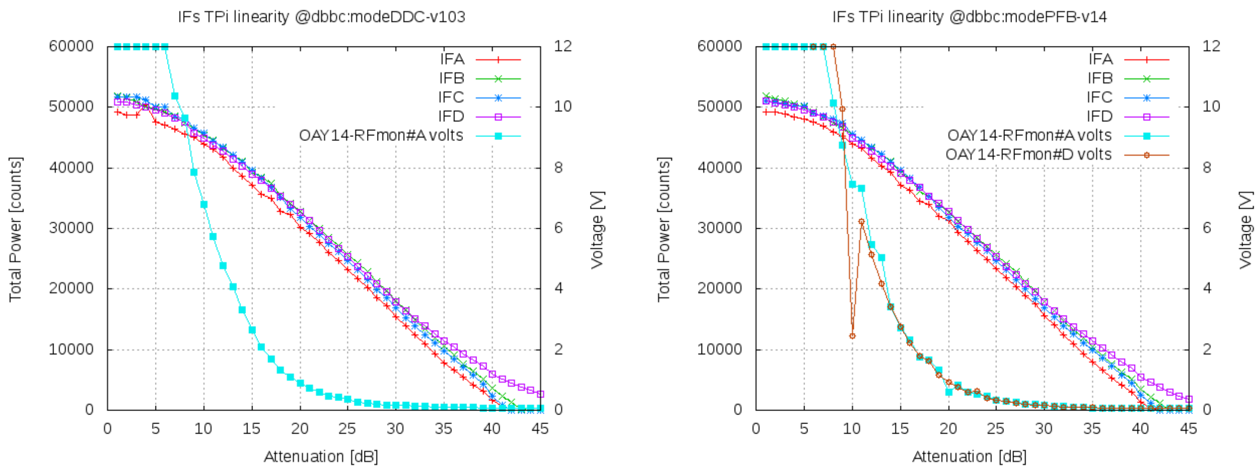

Figure 6: *Power detection in arbitray units and voltage as a function of input power. Left panel: DDC mode (firmware v103). Right panel: PFB mode (firmware v14)*

Obviously both figures show the same results since the CoMos do not depend on the DBBC personality. However this identical behaviour allows to check the performance of the firmware in both cases. We suspect that previous versions of the PFB and DDC mode may not produce stable power detection results and therefore useful measurements. The figures demonstrate that power detection is logarithmic and the range of linearity goes from 5000 to 45000 counts. An optimum value for the input signal power seems to lay between 38000 and 45000 counts since it provides enough power for the ADB and does not saturate the wide band detectors. In principle we have chosen 38000 as the value to use for the automatic gain control in both modes.

We have also used narrow band detections at the CORE boards in both modes. The DDC mode was set to a manual gain value of 25, whereas no manual value is setable for the PFB mode. Results are summarized in Figs. 7 and 8.

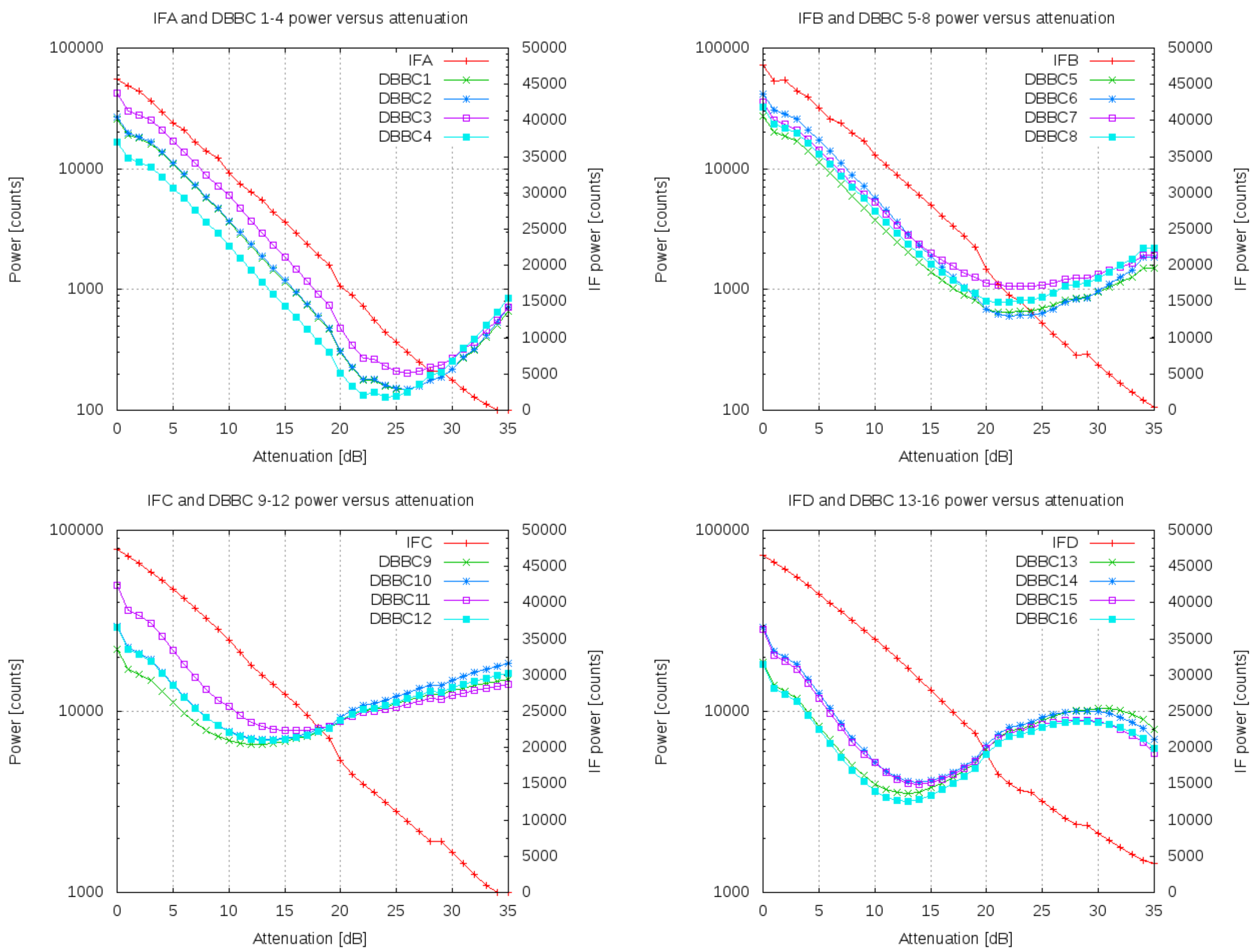

Figure 7: *Power detection in the four IFs and BBC channels 1 to 16. The scale is logarithmic (left y axis) for individual channels and linear (right y axis) for the IF power counts. The dual scale mode allows to compare the regime at which all detectors work linearly*

We have used two different power scales to display the results in DDC mode for all channels: the total IF power is in a linear scale since its detection is logarithmic and the attenuation of the input power is also done in logarithmic steps. The power detected for individual channels is in a logarithmic scale because the detection is linear. These two scales allow to compare the linearity of both detections at a single glance.

There seems to be a different behaviour between COREs 1 and 2 (IFs A and B) and COREs 3 and 4 (IFs C and D). The linearity for the former pair is larger; the input power ranges from 15000 to 50000 counts. Input power below 15000 counts produces non expected results in COREs 1 and 2. CORE 1 generates a decreasing count level down to 10000 counts (according to IFA detector) as power decreases, but below the latter value the detected power begins to increase as power decreases. CORE 2 shows the same behaviour but the turning point happens at 15000 counts (according to IFB detector). As a matter of fact the function that relates detected power with input power for COREs 1 and 2 show a similar behaviour but the slope is higher for the former.

COREs 3 and 4 show a worse behaviour: the linearity range is much more reduced; it goes from 45000 counts to 30000 counts. Signals with an input power lower than 30000 counts according to the wide band detector, cause the individual channel detections to behave in a way opposite to what is expected: the detected power increases as the input power increases. Furthermore, CORE 4 shows a variable behaviour in which the function has two increasing slopes and one decreasing slope.

We believe that this behaviour strongly limits the radiometry capabilities of the DBBC when working in DDC mode and the power level is below 35000 counts. We also find quite surprising the difference in behaviour between COREs. As a future test we intend to exchange the order of the COREs in the stack to check if it is associated with particular COREs or with its position in the stack.

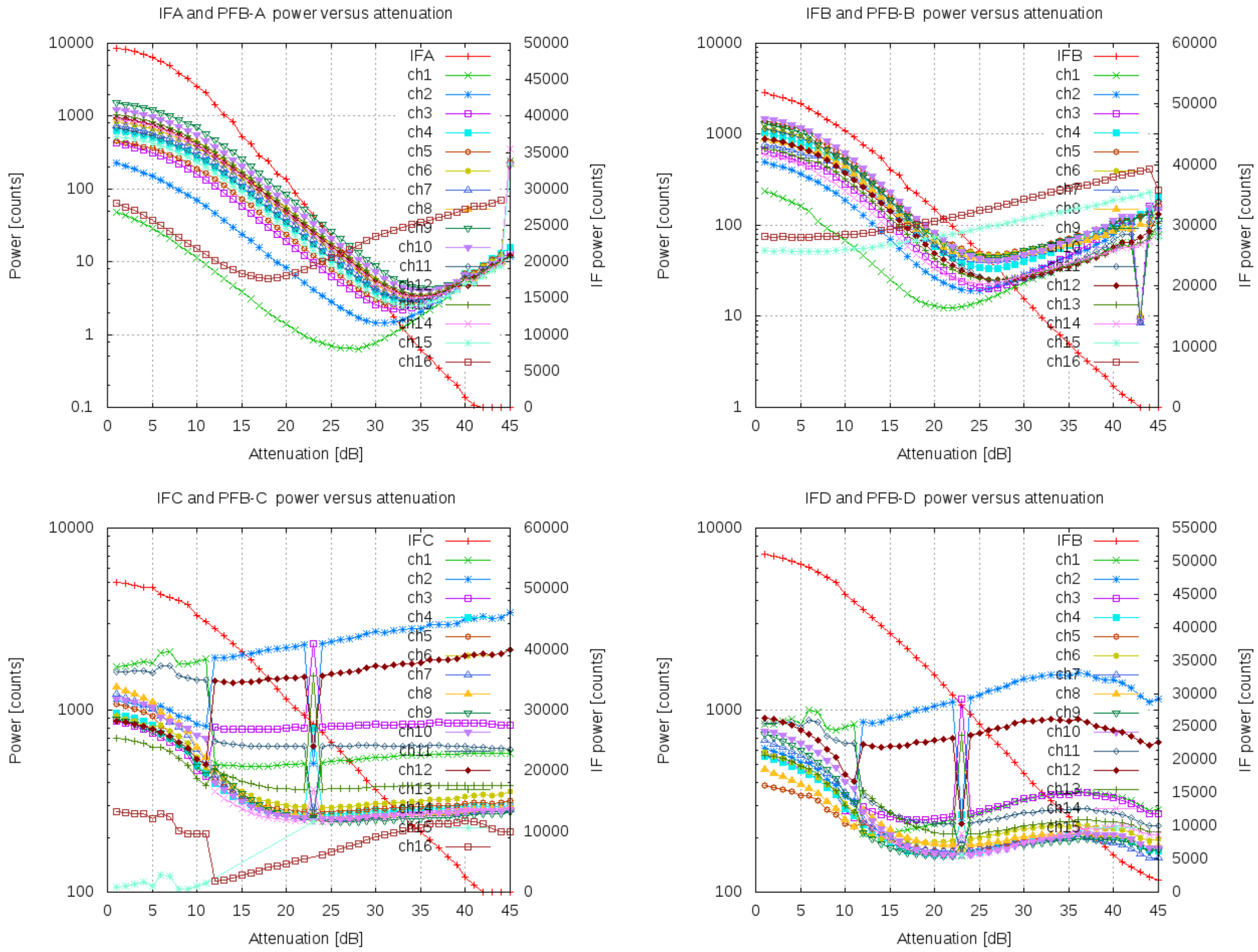

Figure 8: *Power detection in the four IFS and PFB channels. The scale is linear in all cases.*

The behaviour of the DBBC in PFB mode is also partially unexpected as seen from Fig. 8. One of the main differences with the DDC mode is the absolute value of the detection. In most cases the detected power goes between 100 and 1600 counts, whereas in the DDC mode the number of counts was close to 40000 counts. These low values decrease the dynamic range and the precission of system temperature measurements. As with the DDC mode there seems to be a different behaviour between COREs 1 and 2, and COREs 3 and 4. The former show a sort of linear behaviour when the input power is between 15000 and 43000 counts (CORE 1) and between 30000 and 40000 counts for CORE2. COREs 3 and 4 show very erratic behaviour. The linearity interval is extremely short: 40000 to 50000 counts for CORE 3 and 39000 to 48000 counts for CORE 4. Taking into account the dispersion of values we have summarized the linearity intervals for the different modes and COREs in table 2.

In all cases of the PFB mode the linearity is too small and may cause calibration problems if the input power changed much.

Power detector	DDC	PFB
IF A wide band	0 - 45000	0 - 45000
CORE 1 narrow band	17000 - 43000	13000 - 43000
IF B wide band	0 - 45000	0 - 45000
CORE 2 narrow band	20000 - 43000	30000 - 45000
IF C wide band	0 - 45000	0 - 45000
CORE 3 narrow band	34000 - 43000	40000 - 50000
IF D wide band	0 - 45000	0 - 45000
CORE 4 narrow band	34000 - 43000	39000 - 48000

Table 2: *Input power regimes, measured in counts, at which the power detection is linear. The narrow band detection is done in the COREs*

COREs 3 and 4 show random behaviours for channels 2 and 12 along the whole input power range and channels 1 and 11 for input powers between 45000 and 50000 counts. Furthermore there seems to be a strong discontinuity (peak in the detected power) for channels 1, 2, 3, 4 and 12 when the input power is close to 28000 counts.

This faulty behaviour may be related to the fact that the OVERFLOW LED (number 5) in CORE boards 3 and 4 is permanently lit in PFB mode. We suspect that these two COREs are not working correctly, or the signal gets strongly degraded after having travelled thorugh the stack.

After reviewing the linearity at the two operating modes, we conclude that it is rather important to use the automatic gain control to keep the input power close to the linear regime (38000 to 43000 counts) and set it to manual when calibration needs to be done. If the input power changes more than 20% while being in manual mode, results may be not trustable.

6 System temperature in parallel within a geodetic session

We have compared the system temperature determined with the DDBC and the VLBA terminal in a regular IVS observation done in X, extended X and S bands (RCP) for 24 hours. We set two computers, one which runs the experiment, and a second one which only executed a "stripped" schedule with the calibration within the "preob". All instructions which commanded the Mark5B and the antenna were removed from the schedule. The same frequency setup was used in both computers. In order to synchronize the radiometry in both computers we tuned the waiting times in "preob" to make coincide total power measurements in the sky, with and without calibration, in both systems. Synchronization for total power measurements between the DBBC and the VLBA was better than 1 second. We only did parallel observations using BBCs 1 to 12, although in the figures below we only show results for BBCs 1 to 8.

6.1 DDC mode, version 103

Figs. 9 and 10 show the results for R1579 using DDC mode version 103. System temperatures for the DBBC do not match those for the VLBA except for channels 4 and 8, for which they give stable and very similar values to VLBA ones. The polarization was RCP in both cases.

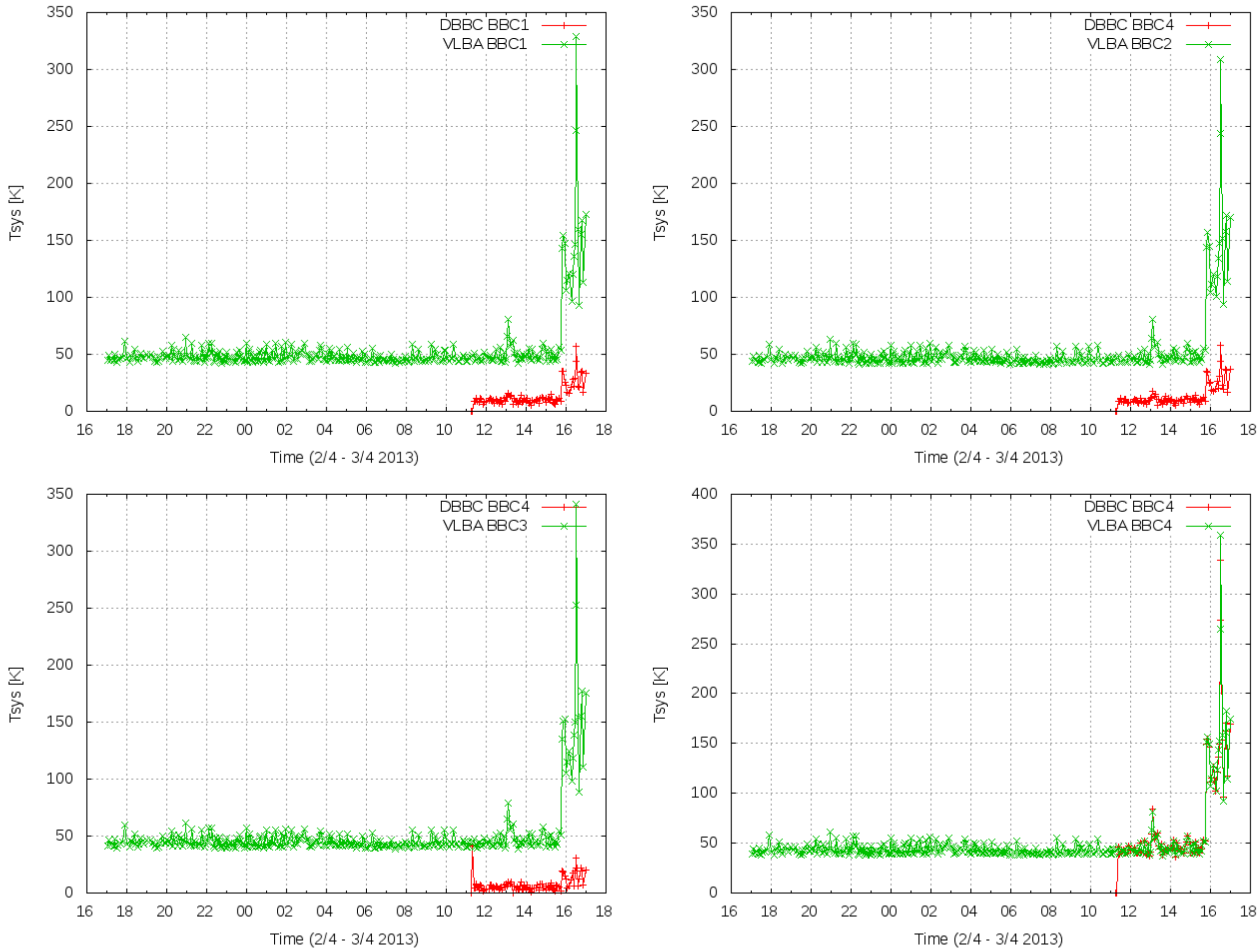

Figure 9: *System temperature for IVS R1579 using the VLBA terminal and the DBBC in DDC mode (firmware version 103) for BBCs 1 to 4.*

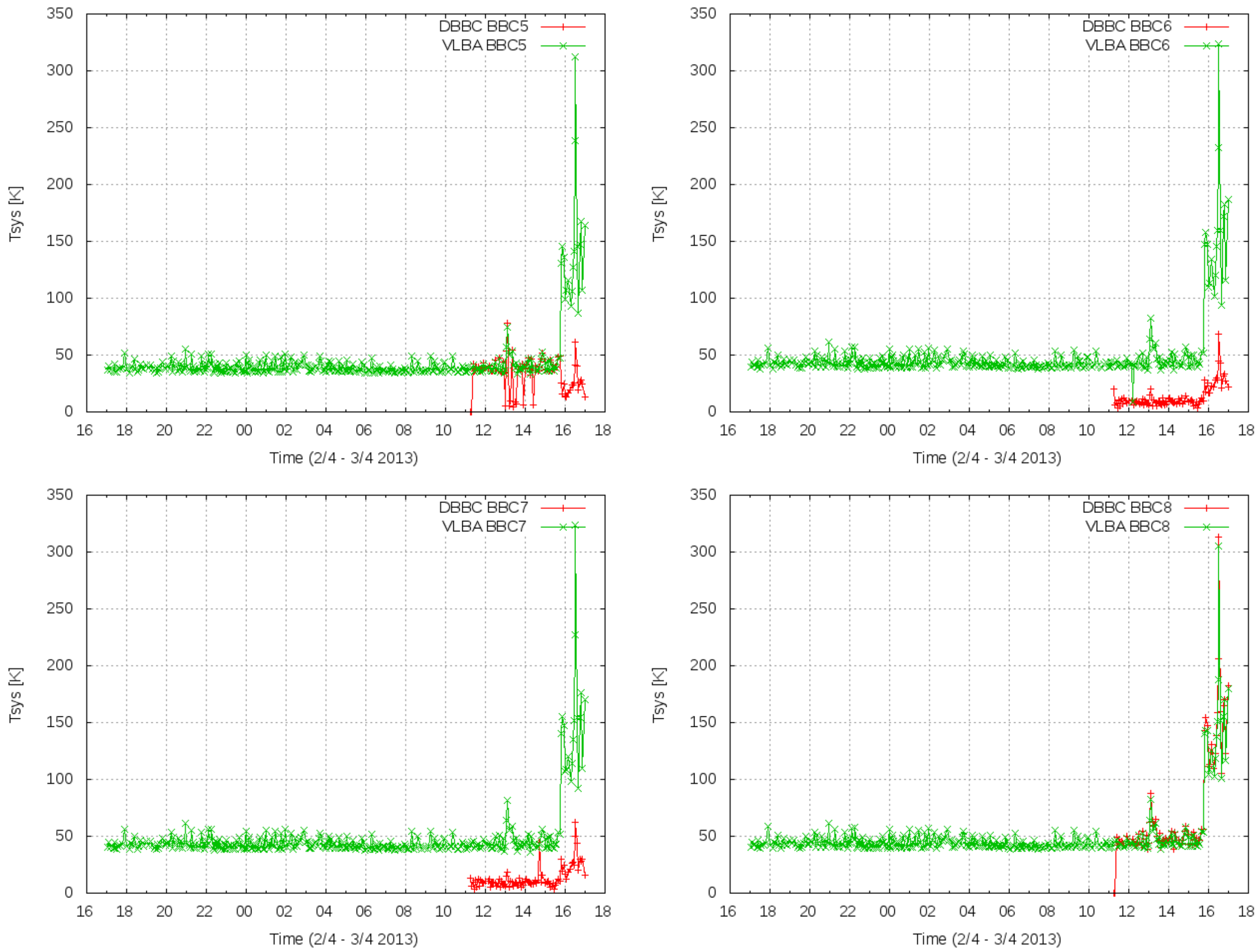

Figure 10: *System temperature for IVS R1579 using the VLBA terminal and the DBBC in DDC mode (firmware version 103) for BBCs 5 to 8.*

6.2 DDC mode, version 102

Figs. 11 and 12 show the results for R4581 using DDC mode version 102. System temperatures for the DBBC and the VLBA match well for all channels between 1 and 8. We also made a comparison with channels in the S band and although they are not included here, they were also in good agreement with data from the VLBA terminal.

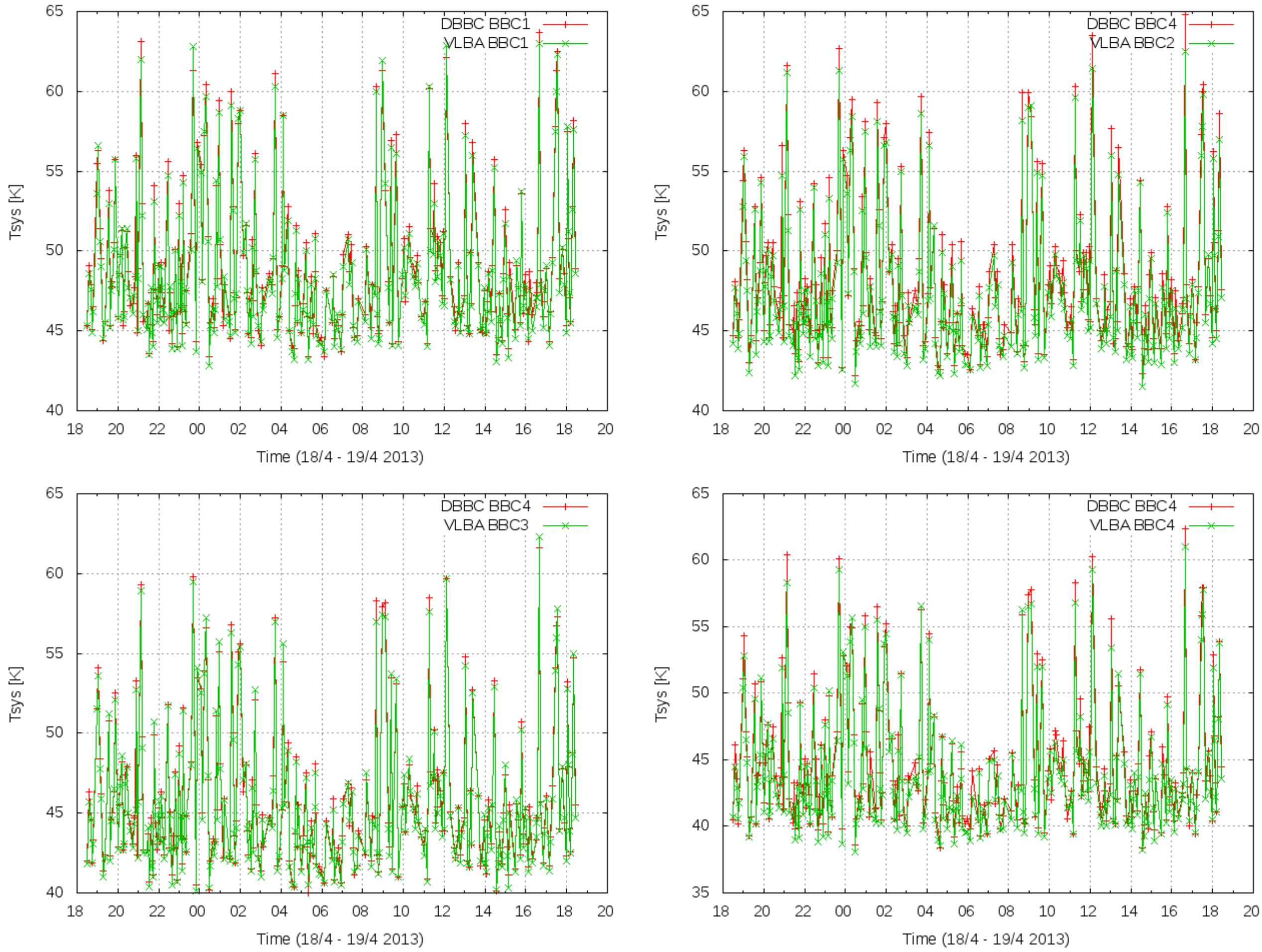

Figure 11: *System temperature for IVS R4581 using the VLBA terminal and the DBBC in DDC mode (version 102) for BBCs 1 to 4.*

7 Testing a calibration scan

Single dish observations in the 40m antenna are periodically calibrated using calibration scans. A calibration scan for cm observing frequencies at 40 m radiotelescope is composed of 5 sub-scans:

- Off source and noise diode off
- Off source and noise diode on

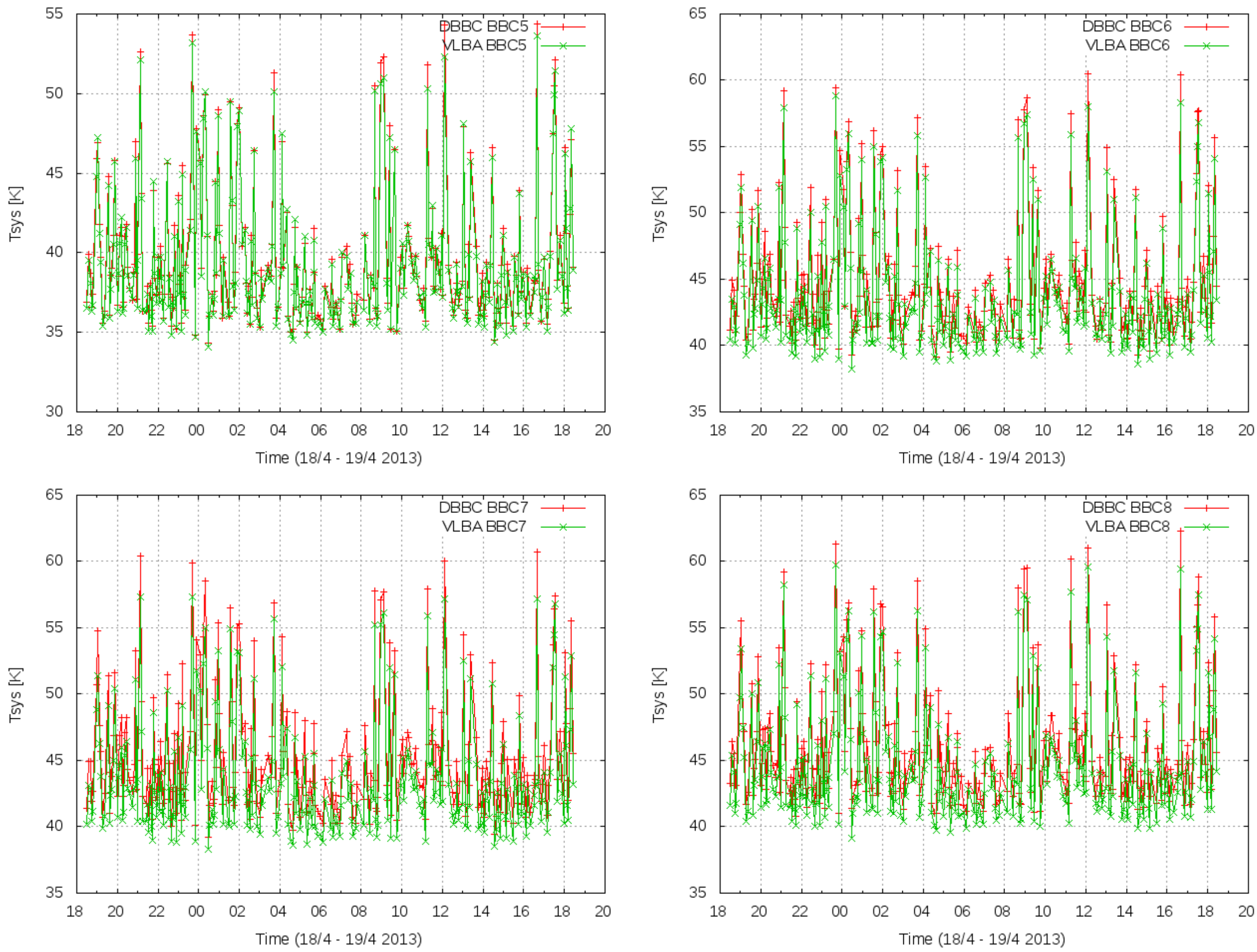

Figure 12: *System temperature for IVS R4581 using the VLBA terminal and the DBBC in DDC mode (version 102) for BBCs 5 to 8.*

- On source and noise diode on
- On source and noise diode off
- Off source and full attenuation (to measure the zero of the detector)

This sequence produces a power graph as a function of time like the one in Fig. 13; all subscans can be clearly distinguished.

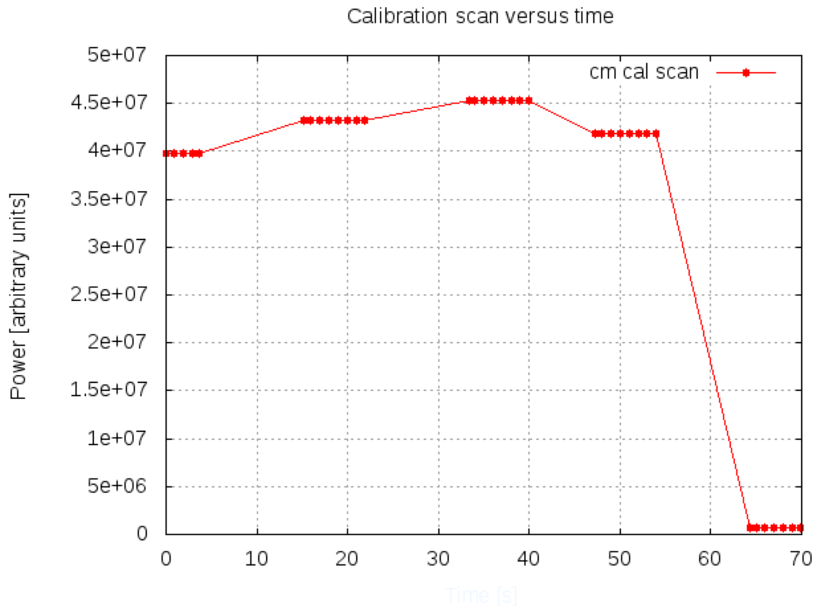

Figure 13: *Typical cm calibration scan with 5 subscans: Off-caloff, Off-calon, On-caloff, On-calon, zero*

7.1 DDC mode, version 103

To check for a correct functioning of the DBBC, we have run a calibration scan at C band, using the four IFs and the two modes: DDC and PFB. We injected the RCP IF signal, after using a 3 dB splitter, into IFs A and C and LCP IF, after a 3 dB splitter, into IFs B and D. Continuum detector OAY14 was connected to "RF Out" output of the IFA module. The setup is shown in Fig. 14. In both cases the IF was set to a manual level of 38000 counts just prior to the scan. Individual channels were in manual mode right before the start of the scan. The results for the DDC mode are summarized in Fig. 15 and for the PFB mode in Fig. 17. The individual channels in DDC mode were set to 650, 670, 690 and 710 MHz.

The calibration scan for the narrow channel detections seems to work correctly in both, DDC and PFB mode provided we discard the last subscan, where we determine the zero of the device. In some channels, the zero produces random values due to the limited number of bits. When the signal is too low or too high the digitized value makes a whole turn starting again.

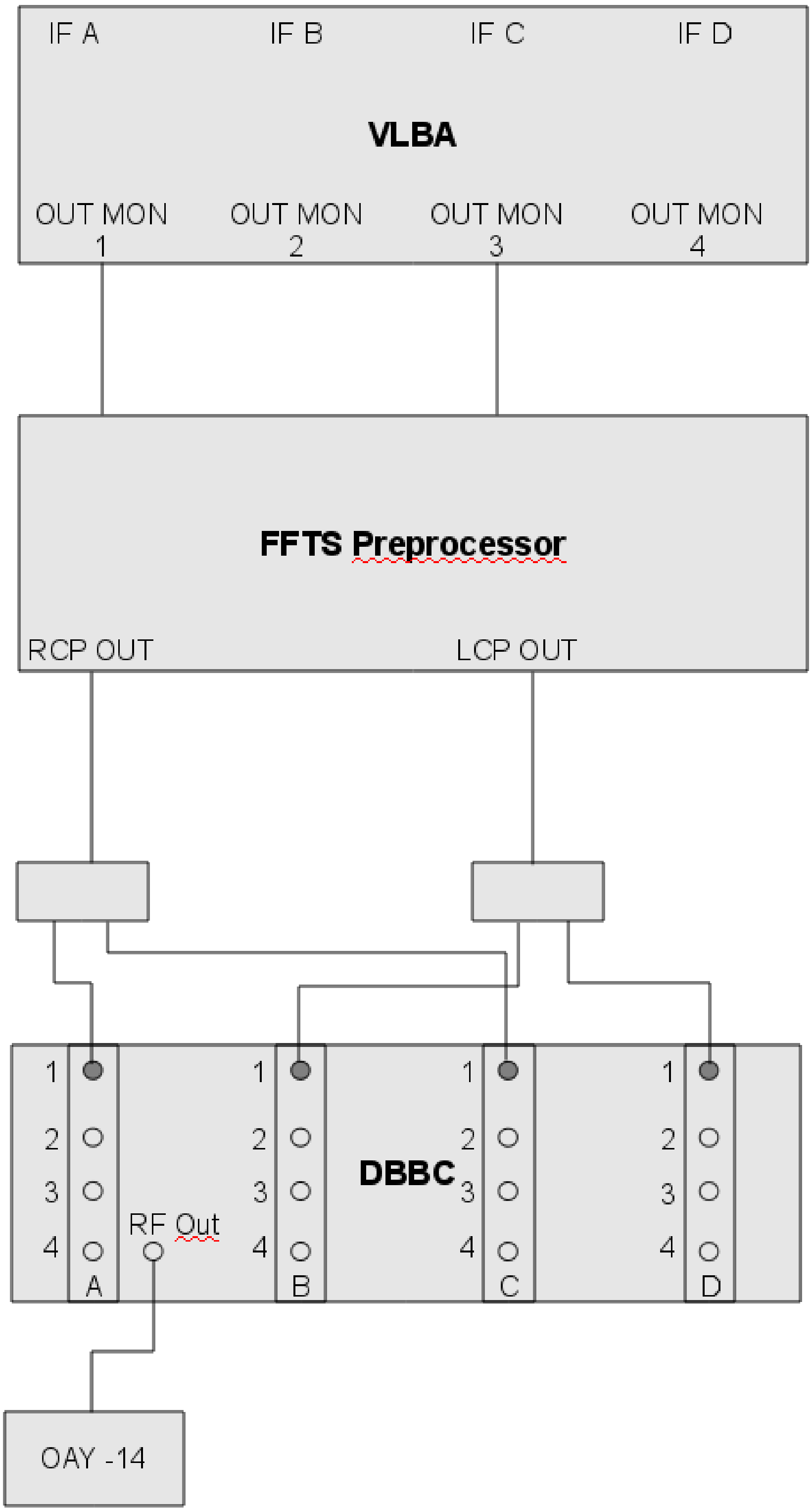

Figure 14: *Setup used to do the calibration scans. The power was measured simultaneously at IFS A and C and B and D. The detected power was also monitored with continuum detector OAY-14 connected to IFA.*

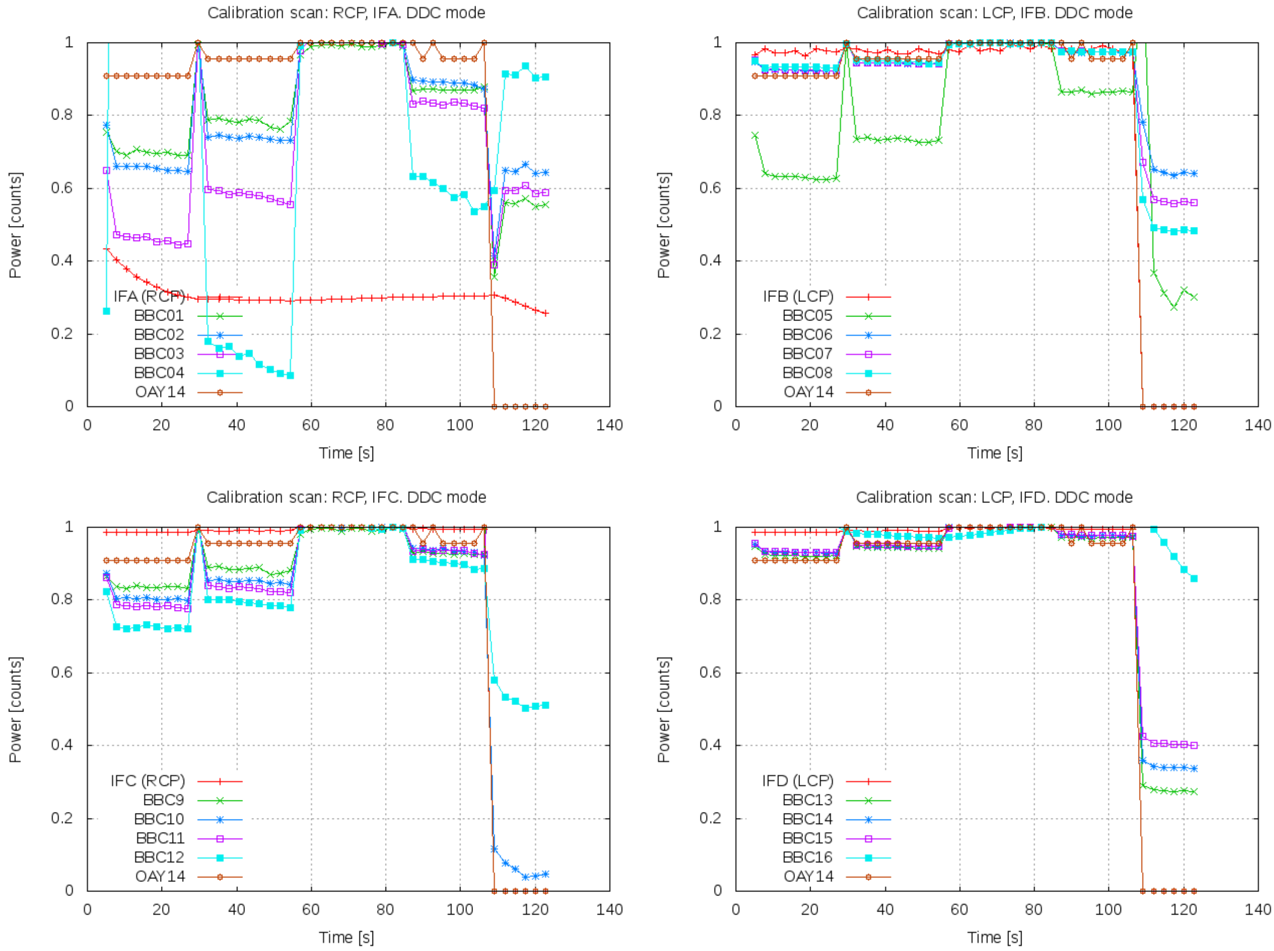

Figure 15: *Calibration scan, DDC mode. Normalized detected power versus time. IF was set to a manual level of 38000 counts and individual channels were set to manual. Panels, upper left: RCP, IFA, lower left: LCP, IFB, upper right: RCP, IFC, lower right: LCP, IFD*

Results from the wide band detector are noisy, probably because the detector is logarithmic and the variation of power across the calibration scan are around 20% at most.

System temperatures determined in DDC mode are summarized in table 3. Each channel displays a value in two columns: the first one is the system temperature determined off the source and the second one on the source. Some channels (BBC04 and BBC16 and IFB) show negative values due to the fact that the total detected power is larger when the noise diode is off than when it is on. This is possibly due to the limited number of bits that causes the count to start when the count goes over the upper limit. The large dispersion, unstability and lack of coincidence between IFs in the measurements make us think that the power detetection system is not working correctly.

Pol.	IF	Wide band		Ch 1		Ch 2		Ch 3		Ch 4		OAY-14	
RCP	A	124.4	41.0	20.6	20.4	20.9	21.5	9.8	13.9	-2.9	3.5	53.2	56.0
RCP	C	114.8	67.7	45.4	38.9	43.5	36.3	41.7	37.3	31.2	22.7		
LCP	B	98.1	-290.0	14.6	17.9	111.7	108.6	122.0	108.2	140.2	115.7		
LCP	D	115.1	131.7	93.8	96.2	132.8	122.0	126.6	128.0	-23.8	-149.3		

Table 3: *System temperature at C band in DDC mode (version 103) determined using a noise diode, off source (left column) and on source (right column). Values are in K*

7.2 DDC mode, version 102

As with firmware version 103 in DDC mode, we have also run a calibration scan at C band, using the four IFs. Measurements were done in two steps, first IFs A and B and in a second round IFs C and D. Continuum detector OAY14 was not connected to any "RF Out" output this time. In both cases the IF was set to a manual level of 38000 counts just prior to the scan. Only one mesaurement per phase was taken. Individual channels were in manual mode right before the start of the scan. The results for the DDC mode are summarized in Fig. 16. The individual channels in DDC mode were set to 650, 670, 690 and 710 MHz.

As with firmware version v103, phases of the calibration scan can easily be distinguished. System temperatures obtained are summarized in table 4. Each channel displays a value in two columns: the first one is the system temperature determined off the source and the second one on the source. System temperatures are much more stable than in version 103. Except for two cases, the system temperatures obtained in the "on" phase and in the "off" phase match quite well.

7.3 PFB mode, version 14

Results from a calibration scan in PFB mode are shown in Fig. 17 and the results for the different channels in table 5.

System temperatures show some dispersion, with some channels displaying negative values. It seems that the first 3 channels produce in both cases, all of the nonsense values (negative ones) and the values that depart most from the average.

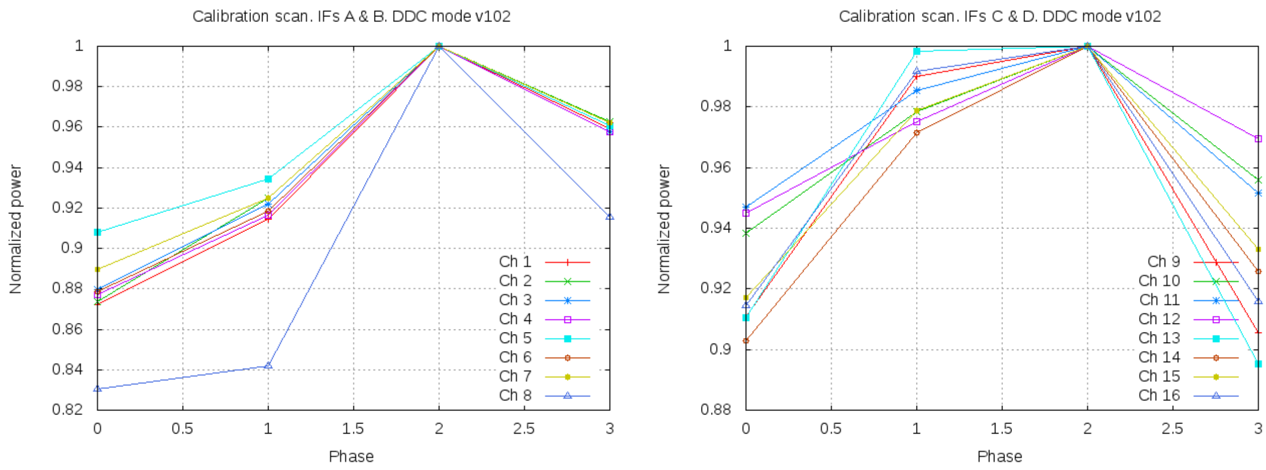

Figure 16: *Calibration scan, DDC mode firmware 102. Normalized detected power versus time. IF was set to a manual level of 38000 counts and individual channels were set to manual. Left panel: RCP (IFA) and LCP (IFB), Right panel: RCP (IFC) and LCP (IFD)*

Pol.	IF	Wide band		Ch 1		Ch 2		Ch 3		Ch 4	
RCP	A	92.6	-211.1	57.7	66.3	47.8	72.6	58.0	63.1	62.4	63.1
RCP	B	46.2	249.3	96.6	68.1	61.1	71.4	70.7	70.8	199.7	30.4
LCP	C	70.4	72.4	32.2	26.9	65.3	60.7	68.8	55.1	87.9	88.6
LCP	D	72.8	67.4	29.1	23.9	36.9	34.9	41.4	39.0	33.1	30.5

Table 4: *System temperature at C band in DDC mode i(version 102) determined using a noise diode, off source (left column) and on source (right column). Values are in K*

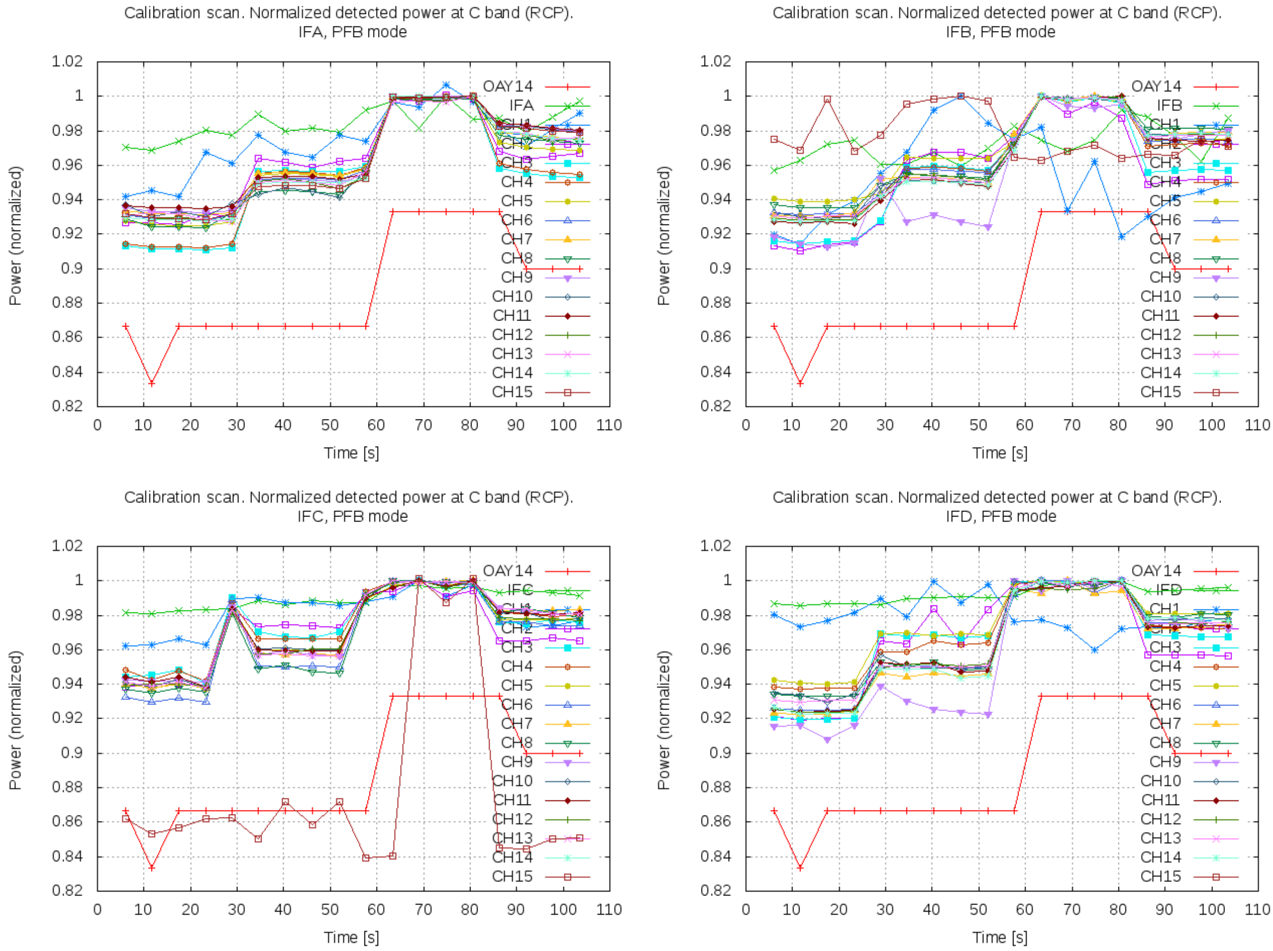

Figure 17: *Calibration scan, PFB mode. Normalized detected power versus time. IF was set to a manual level of 38000 counts and individual channels were set to manual. Panels, upper left: RCP, IFA, lower left: LCP, IFB, upper right: RCP, IFC, lower right: LCP, IFD. The last subscan was suppressed*

Channel	RCP		LCP	
1	-840.0	212.8	37.7	-118.4
2	98.1	84.2	38.9	-242.3
3	55.9	58.8	44.1	69.5
4	58.8	61.8	53.7	68.4
5	85.9	90.6	83.8	112.6
6	106.5	117.6	97.9	125.5
7	110.4	117.6	95.8	119.0
8	122.1	110.4	123.0	143.5
9	137.2	148.6	128.0	166.2
10	181.7	171.4	186.5	166.6
11	140.4	152.8	119.5	132.2
12	117.0	114.2	100.6	116.0
13	122.5	125.4	94.1	137.2
14	117.9	114.0	114.0	131.5
15	134.6	142.2	103.8	145.3
1	690.8	119.1	75.2	-368.8
2	110.2	104.6	-676.5	15.8
3	76.9	82.1	427.3	-714.3
4	99.3	121.5	53.5	65.2
5	106.0	133.3	49.2	84.6
6	116.5	126.5	93.2	104.3
7	123.9	105.9	84.7	149.6
8	137.2	166.7	99.2	111.7
9	233.7	149.5	117.3	103.3
10	171.3	147.0	152.5	178.1
11	117.6	119.1	315.7	117.2
12	126.2	141.7	156.5	134.5
13	120.4	123.5	103.3	121.9
14	141.2	149.8	87.1	137.5

Table 5: *System temperature at C band in PFB mode determined using a noise diode, off source (left column) and on source (right column). Values are in K. The first block of lines is for IFs A and B and the scond block for C and D*

8 Conversion factor in the Field System

The conversion factor is a constant to be applied when converting power from logarithmic units to natural units. These 4 numbers (one per CoMo) can be set in control file `/usr2/control/equip.ctl` and by default their value is 15000.

The Fieldsystem makes the following conversion when computing the system temperature (T_{sys}):

$$T_{sys} = T_{cal} \frac{P_{caloff}}{P_{calon} - P_{caloff}} \tag{1}$$

where T_{cal} is the calibration temperature, and P_{calon} and P_{caloff} are the detected power (in natural units) when the noise diode is on and off respectively. According to the Field System, when using the wide band detectors in the CoMos, the power with the diode on and off is converted to natural units as follows:

$$P_{calon} = 65535\, 10^{(c-65535)/f} \tag{2}$$

where c is the logarithmic power in arbirtray units, also known as counts which range from 0 to 65535. The upper limit comes from using 16 bit to quantize the signal ($2^{16} = 65536$). In principle the conversion factor should not be very important but it really makes a difference as shown by Fig. 18 where we display several curves with different conversion factors.

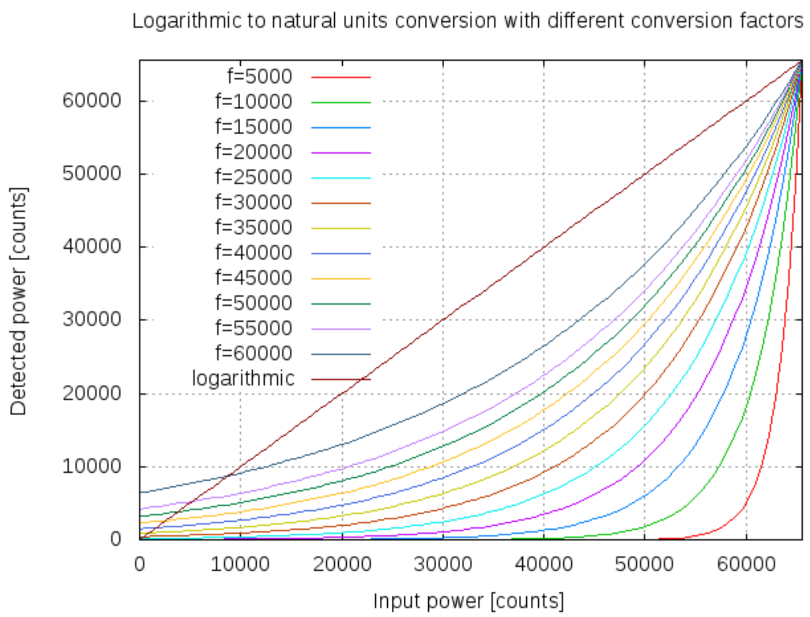

Figure 18: *Conversion between logarithmic counts and linear counts with different factors*

The conversion factor depends on each CoMo. In order to measure the optimum value, a calibrated signal was injected into the IF of each CoMo, its IF gain control was set to manual using different attenuation values, and the detected power was measured using the wide band power detector. We applied the conversion in equation 2 and compared the value obtained with that one from an HP8562A spectrum analyzer connected to the "RF Mon" output. Using 1 MHz frequency resolution the total power detected in a band 500 MHz wide, is:

$$P_{500MHz} = P_{1MHz} + 10\log(500) = P_{1MHz} + 27 \tag{3}$$

3 dB should be added to the power detected by the spectrum analyzer due to the usage of one power splitter to compare it with the detected power. The measured power at the spectrum analyzer when the attenuator's noise source is set to 20, is -42 dBm/MHz which corresponds to 45 nW. In order to get the power of the input signal an additional 3 dB should be added.

Figs. 19 to 22 show the results. Each figure shows the normalized detected power (number of counts/65535) of the input signal once a conversion factor has been applied to convert from logarithmic to natural units as a function of the power of the input signal in dBm. The latter was measured with the spectrum analyzer. The normalized detected power (ouput power/input power) as detected by the spectrum analyzer in watts is also displayed with a red curve. The optimum conversion factor is that one whose curve matches the red one.

As we can see none of the curves completely matches the red curve, since saturarion happens much before than 65535 counts. However we can estimate the best conversion factor by comparing the curves below 48000 counts (-5 dBm). The optimum values are summarized in table 6 and are very close to 15000.

	CoMo A	CoMo B	CoMo C	CoMo D
factor	16000	17000	16000	15000

Table 6: *Recommended conversion factors for the four IF modules.*

9 Conclusion

Firmware version 103 for DCC mode produces random system temperatures values and hence we discard its usage. Currently, in april 2013, version 102 is the recommended firmware version since radiometric measurements show good agreement with those from the VLBA terminal. Although the internals of version 103 are unknown, it seems that the main cause for the unstable values comes from the usage of a limited number of bits (16) and its behaviour when the values reach the maximum. The number that gives the power is undetermined and renders unreliable system temperatures.

Version 14 for the PFB mode generates random values for Tsys and a very short interval where linearity is avilable. There are significative differences between IFs A, B, C and D. We do not know if this version is also affected by the same numeric problem as DDC version 103. In any case we suspect that the signals may get degraded along the stack. Hardware modifications proposed and described by M. Wunderlich for the ADB boards should be applied to check if the linear regime increases and system temperatures get more stable.

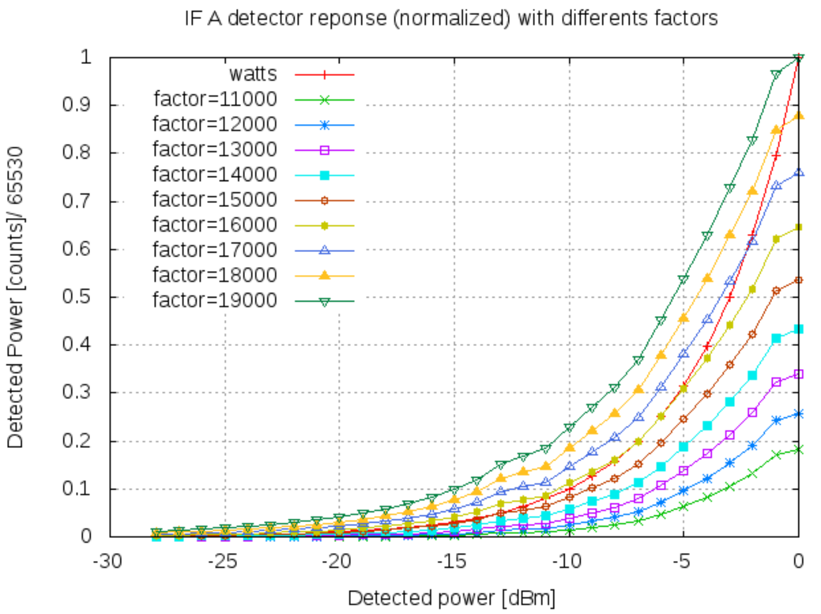

Figure 19: *Normalized detected power versus detected power in dBm using a spectrum analyzer. IF A*

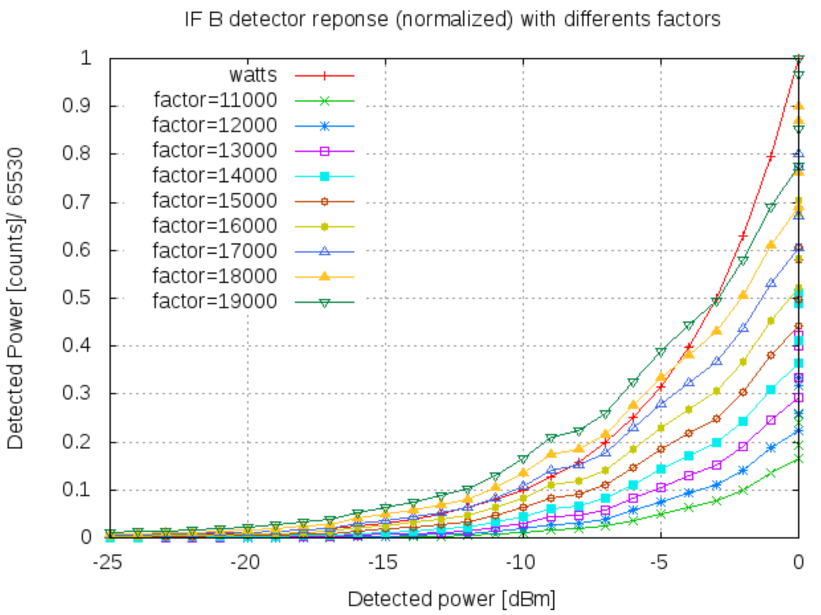

Figure 20: *Normalized detected power versus detected power in dBm using a spectrum analyzer. IF B*

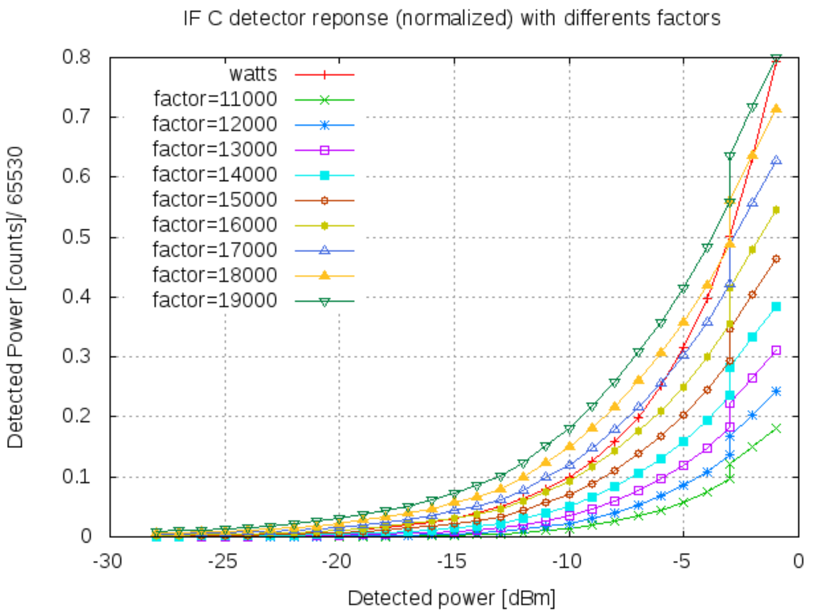

Figure 21: *Normalized detected power versus detected power in dBm using a spectrum analyzer. IF C*

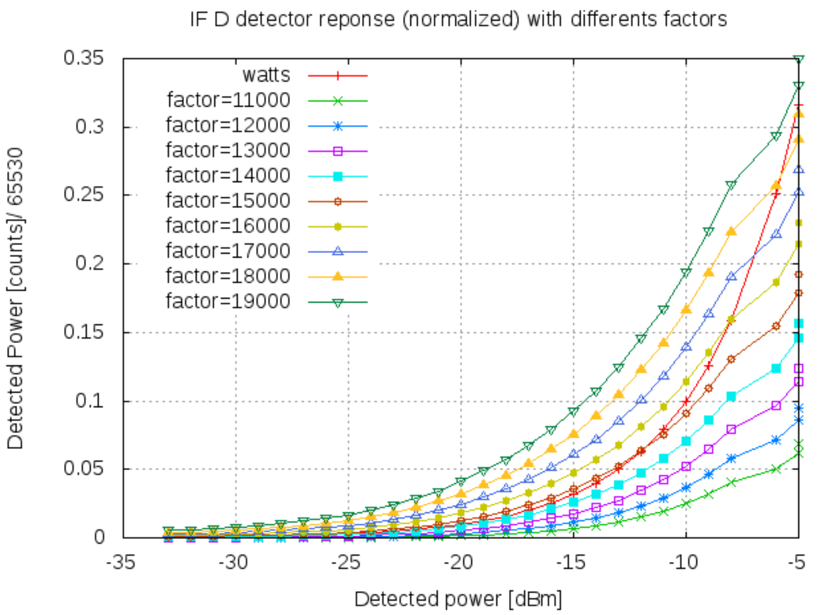

Figure 22: *Normalized detected power versus detected power in dBm using a spectrum analyzer. IF D*

References

[1] P. de Vicente *DBBC installation and tests at the 40 m radiotelescope*, IT-OAN, 2011