Metamorphic HEMT Technology for Low-noise Applications

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ABSTRACT

Different noise sources in HEMTs are discussed, and state-of-the-art low-noise amplifiers based on the Fraunhofer IAF 100 nm and 50 nm gate length metamorphic HEMT (mHEMT) process are presented. These mHEMT technology feature an extrinsic f_T of 220 / 375 GHz and an extrinsic transconduction $g_{m,\,max}$ of 1300 / 1800 mS/mm. By using the 50 nm technology several low-noise amplifier MMICs were realized. A small signal gain of 21 dB and a noise figure of 1.9 dB was measured in the frequency range between 80 and 100 GHz at ambient temperature. To investigate the low temperature behaviour of the 100 nm technology, single 4 * 40 µm mHEMTs were integrated in hybrid 4 - 8 GHz (Chalmers) and 16 - 26 GHz (Yebes) amplifiers. At cryogenic temperatures noise temperatures of 3 K at 5 GHz and 12 K at 22 GHz were achieved.

I. INTRODUCTION

Low-noise amplifiers find many applications in science and technology. They are used for the detection of weak signals in radio astronomy, wireless communication, radar or radiometer systems. All noise added to the incoming signal by the amplifier circuit degrades the signal-to-noise ratio which determines whether a signal can be detected or not. For higher frequencies where the 1/f-noise is insignificant, amplifiers with the lowest noise figures are based on advanced high electron mobility transistors (HEMTs). The reason for the low internal HEMT noise is due to the high electron mobility in the undoped channel. This high mobility is a result of the low scattering probability of the electrons. Other device parameters which are important for the noise behaviour are: contact resistance, gate-line resistance or gate leakage current. These parameters have to be taken into account for a proper transistor design.
A further suppression of electron scattering and therefore reduction of the noise figure can be achieved by cooling down the HEMTs. Because of advances in cooling technology regarding cost and size, cryogenic operation of HEMTs for ultra low-noise amplifiers might find wider distribution in the near future. The lower ambient temperature of the transistor does not only change the channel mobility but also influences other device parameters which has to be considered.

II. TECHNOLOGY

The results presented in this paper are based on mHEMT technologies with 50 nm and 100 nm gate length developed at the IAF [1, 2]. The mHEMT layers are grown on 4” semi-insulating GaAs wafers by molecular beam epitaxy (MBE). For the metamorphic buffer a linear $In_xAl_{0.48}Ga_{0.52-x}As$ ($x = 0 \rightarrow 0.52$) transition is used. In the 100 nm gate length technology the electrons are confined in an $In_{0.65}Ga_{0.35}As/In_{0.53}Ga_{0.47}As$ composite channel, which was chosen to increase the breakdown voltage. The split channel is confined by $In_{0.52}Al_{0.48}As$ barriers. The layer sequence is capped with a highly-doped $In_{0.53}Ga_{0.47}As$ layer. For the 50 nm mHEMT the gate-to-channel separation was decreased to get a better aspect ratio and therefore to suppress short-channel effects. In addition the In content of the upper composite channel layer was increased to 80% to reduce source resistance. Typical electron densities and hall mobilities are $n_e = 3.8 \cdot 10^{12}$ cm^{-2} and $\mu_e = 11000$ cm^2/Vs for the 100nm and $n_e = 4.2 \cdot 10^{12}$ cm^{-2} and $\mu_e = 11800$ cm^2/Vs for the 50nm technology. A wet chemically mesa etch process is used for device isolation. The InGaAs channel layer is under-etched to avoid contact between the conducting InGaAs channel material and the gate metallization crossing the mesa edge in order to avoid gate leakage currents. Electron beam evaporated GeAu layers are used for the Ohmic contacts which are alloyed at 300°C on a nitrogen purged hot plate.

Tab. 1: Electrical Parameters of mHEMT technologies at ambient temperature.

	50 nm	100 nm
In content	80%	50%
R_c (Ωmm)	0.07	0.05
R_s (Ωmm)	0.15	0.23
R_g (Ω/mm)	250	400
$I_{D,\,max}$ (mA/mm)	1200	900
BV_{BD} (V)	2.5	4
$g_{m,\,max}$ (mS/mm)	1800	1300
f_t (GHz)	375	220
f_{max}	≈ 500	300

The T-gates are defined by 100 kV electron beam lithography using a three-layer resist (PMMA) for the 100 nm and a four-layer resist for the 50 nm gates. The gate recess is etched with a succinic acid based solution. The gate metallization consists of a Pt-Ti-Pt-Au layer sequence. In the 50 nm technology the gate is encapsulated in BCB to reduce the parasitic gate capacitances. The devices are passivated with a 250 nm thick CVD deposited SiN layer used as dielectric layer for the MIM capacitors. Further passive elements are NiCr thin film resistors, an electron beam evaporated Au based interconnection layer and a 2.7 µm thick plated Au layer in airbridge technology. Furthermore, the wafers are thinned down to 50 µm. Through-substrate vias with 20 µm contact diameter to the front side are processed by dry etching. Finally, the wafer backside is Au plated. Some important electrical parameters of the 50 nm and 100 nm mHEMTs are listed in table 1.

III. RESULTS

Noise is created by fluctuations due to scattering within the charge transport. Scattering generates electric resistance which is why low access resistances are necessary for low noise devices. The optimized Ohmic contact resistances are as low as 0.07 and 0.05 Ω*mm, respectively. For the same reason a low gate-line resistance is desirable. Realizing a low gate-line resistance without degrading the high frequency performance due to increased parasitic capacitances of the gate head was the main problem in the noise optimization of the 50 nm process. Using an optimized gate cross section a line resistance of 250 Ω/mm was achieved. This is even lower than the 400 Ω/mm of the 100 nm technology.

The correlation between gate-line resistance and minimum noise temperature T_{min} of HEMTs is given by [3]:

$$T_{min} \sim \frac{f}{f_{Ti}} \sqrt{R_g + R_{gs} + R_s} \qquad (1)$$

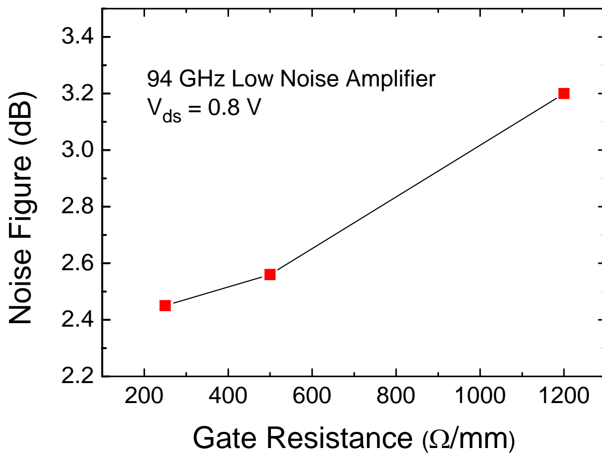

Fig. 1: Noise figure of 94 GHz amplifier MMICs as a function of gate resistance at ambient temperature. With decreasing gate-line resistance the noise figure is significantly reduced.

Where f_{ti} is the intrinsic transit frequency and R_g, R_{gs}, R_s are the gate, channel and source resistances. To investigate the influence of the gate-line resistance on the MMIC noise figure a W-band LNA circuit was chosen. On a single 50 nm wafer, mHEMT devices with three different gate cross sections and therefore three different gate-line resistances were processed to avoid wafer-to-wafer variations. The fabricated LNAs were measured at $V_{ds} = 0.8$ V which is the optimum low-noise bias point of the 50 nm technology. In agreement with formula (1) there seems to be a saturation of the LNA noise figure for low gate-line resistances (Fig. 1). The drain current at this low-noise bias point was $I_d = 30$ mA. All measurements were performed at room temperature (T = 293 K).

As a matter of course the LNA noise figure does not only depend on the transistor but also on the circuit design. A coplanar two-stage LNA circuit was developed, meeting the requirements of W-band high resolution imaging applications for low noise figures, broadband gain characteristics and low power consumption. Fig. 2 shows a chip photograph of the realized amplifier MMIC using 50 nm mHEMT technology. The LNA was designed to achieve high gain in combination with a low noise figure, and covers a chip area of only 0.75×1.5 mm^2.

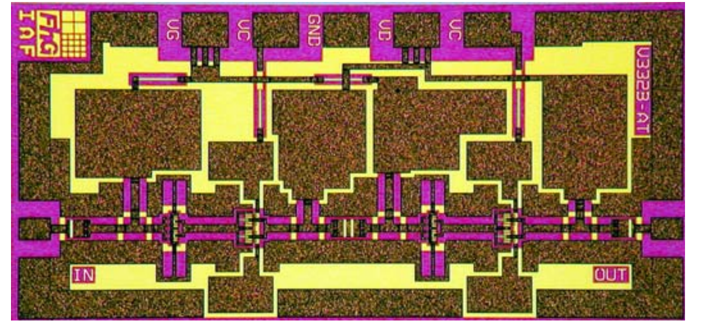

Fig. 2: Chip photograph of 50 nm gate length W-band LNA MMIC.

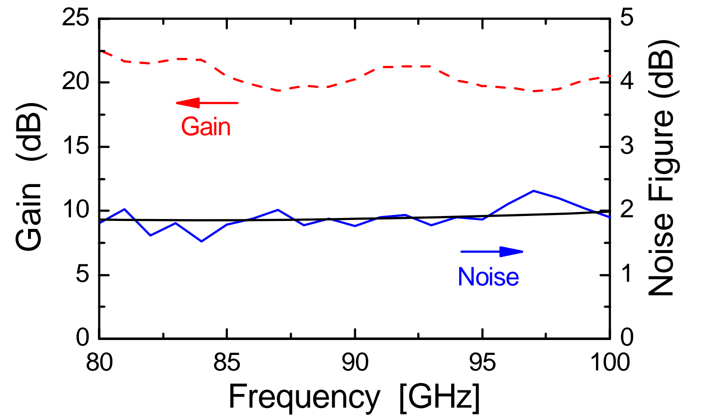

Fig. 3: Low-noise amplifier in 50 nm mHEMT technology demonstrating a noise figure of 1.9 dB in combination with a small signal gain of more than 20 dB between 80 and 100 GHz at ambient temperature.

Tab. 2: Gain and noise figure of 94 and 210 GHz MMICs in 50 and 100 nm mHEMT technology

	gain (dB) @ 94 GHz	noise (dB) @ 94 GHz	gain (dB) @ 210 GHz	noise (dB) @ 210 GHz
50 nm	20	1.9	17.5	4.8
100 nm	22	2.5	18	7.4

Therefore a cascode configuration, consisting of a series connection of one HEMT in common source and one in common gate configuration was utilized. The integrated transistors have a gate width of 4 × 15 µm. To overcome stability problems of the cascode transistor, a short section of coplanar transmission line was integrated between the transistor in common source and the transistor in common gate configuration. The on-wafer measured small-signal gain and the noise figure of the low-noise amplifier MMIC are shown in Fig. 3. A linear gain of more than 20 dB and an average noise figure of 1.9 dB were obtained between 80 and 100 GHz by applying a drain voltage of $V_{ds} = 1.4$ V, a second gate voltage of $V_{g2} = 0.95$ V and a gate voltage of $V_g = 0.2$ V.

To compare the noise performance of the 50 nm and the 100 nm mHEMTs, low-noise amplifiers at 94 GHz and 220 GHz were realized in both technologies (Tab. 2). Each MMIC design was optimized for the used transistor gate length with the help of circuit simulations. All amplifier circuits demonstrate more than 17 dB gain, therefore the influence of the gain on the noise performance is negligible. To our knowledge the 1.9 dB noise figure of the 50 nm technology at 94 GHz (Fig. 3) and 4.8 dB at 210 GHz [5] are the lowest ever published values for these frequencies. The lower noise figure of the 50 nm mHEMT is in agreement with formula (1) due to the higher transistor f_{Ti} of the 50 nm technology.

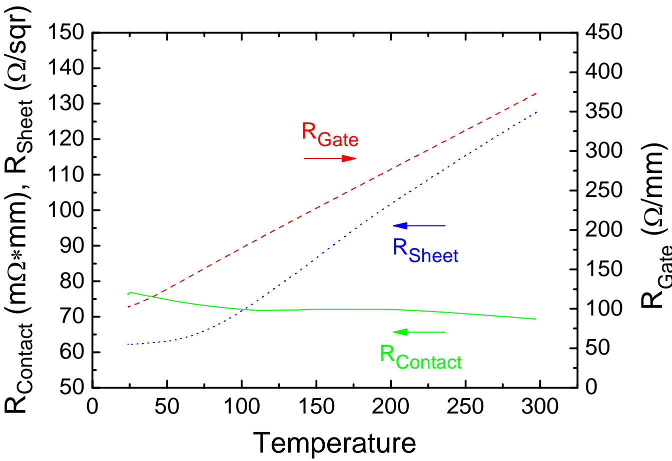

Fig. 4: Temperature dependency of contact, sheet and gate-line resistance of the 100 nm mHEMT technology. The contact resistance at 15 K is only slightly increased.

Nevertheless this is not self-evident because scattering in the channel due to electron-hole pair generation has a higher probability for the 50 nm process with the lower band gap energy due to the 80 % In content channel. The lowest noise figures of amplifiers are obtained at cryogenic temperatures. When electron-phonon scattering is reduced, the semiconductor sheet, and the metal gate-line resistances become lower. In addition, the noise influence of the gate leakage current due to thermal emission of electrons over the Schottky barrier is suppressed. On the other hand the lower thermal emission can drastically increase the contact resistance. The measured temperature dependency of contact, sheet and gate-line resistance for the 100 nm IAF mHEMT is presented in Fig. 4 down to 15 K.

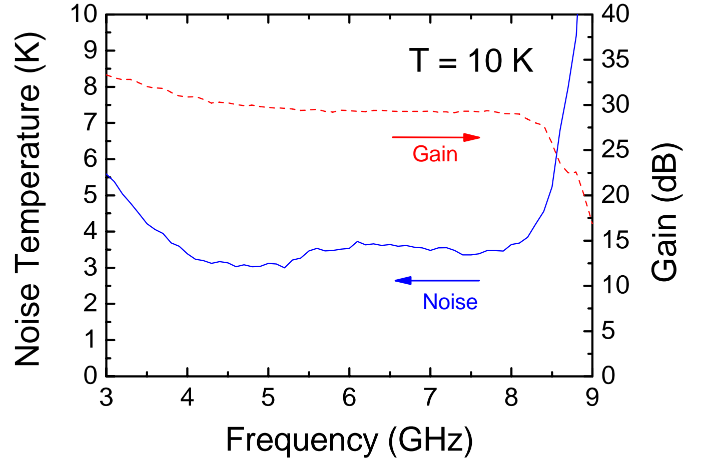

*Fig. 5: Noise temperature and gain of a hybrid 4-8 GHz amplifier at T = 10 K. A 4 * 40 µm mHEMT device with 100 nm gate length was used.*

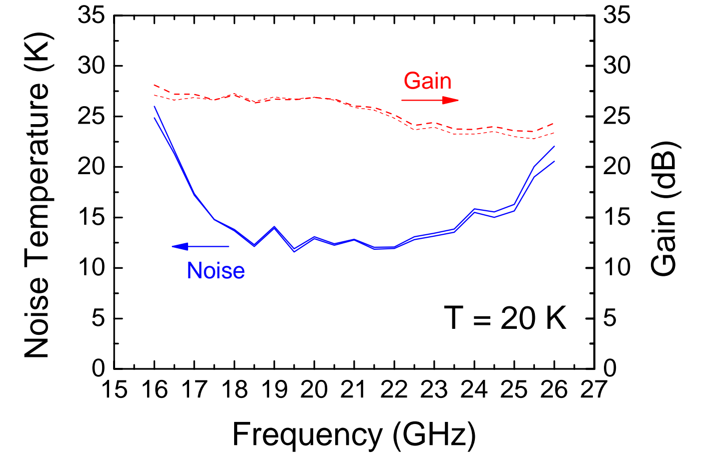

Fig. 6: Noise temperature and gain of hybrid 16 - 26 GHz amplifiers at 20 K. The two curves correspond to two different 4 x 40 µm mHEMTs with 100 nm gate length mounted in the same amplifier module.

It should be taken into account that the sheet resistance includes the contribution of the highly doped cap layer where the carrier mobility is not limited by phonon scattering and therefore nearly temperature independent. The contact resistance shows only a slight increase by approximately 10 %.

To investigate the cryogenic low-noise behaviour of the 100 nm mHEMT technology, single 4 * 40 µm devices were integrated in the first stage of hybrid 4 - 8 GHz (Chalmers) and 16 - 26 GHz (Yebes) amplifiers for cryogenic S-parameter and noise measurements. At 5 GHz and 22 GHz the measured noise temperatures were 3 K (0.045 dB) and 12 K (0.176 dB), respectively (Fig. 5 and Fig. 6). These results are very comparable to the lowest noise temperatures achieved with InP based HEMTs [6, 7]. This is the first time that state-of-the-art cryogenic noise performance could be demonstrated for a metamorphic HEMT technology.

IV. CONCLUSION

50 nm and 100 nm metamorphic HEMT technologies are well suitable for the realization of low-noise amplifiers up to frequencies beyond 200 GHz. After optimization of the gate cross section concerning gate-line resistance and parasitic capacitances a significant improvement of the 50 nm noise performance over the 100 nm technology was achieved. Based on the 50 nm technology a 94 GHz LNA MMIC with more than 20 dB gain and room temperature noise figure of only 1.9 dB was realized. Furthermore the suitability of the 100 nm mHEMT technology for cryogenic applications was investigated. By cooling down to temperatures around 20K and even below, the hybrid amplifiers achieved noise temperatures of 3 and 12 K at 5 and 22 GHz, respectively. These results are very comparable to the best results achieved with cryogenic InP HEMT technologies.

V. ACKNOWLEDGEMENTS

This work was supported by the German Federal Ministry of Defence (BMVG) and the Bundeswehr Technical Center for Information Technology and Electronics (WTD81). We express our gratitude to our colleagues at IAF for their excellent contribution during epitaxial growth and wafer processing.

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